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VOICE OF ENGINEER

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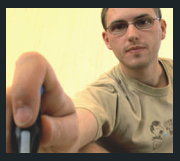


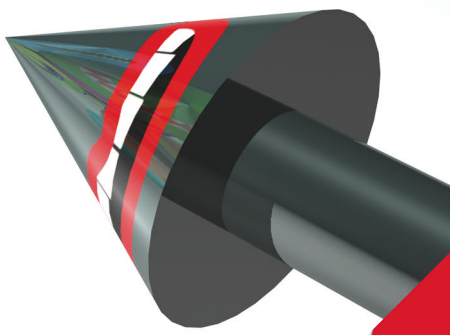


## INTEGRATION IN THE OTHER DIRECTION

Page 24

## RECOGNIZING TECHNOLOGY'S INFLECTIONS

Page 19





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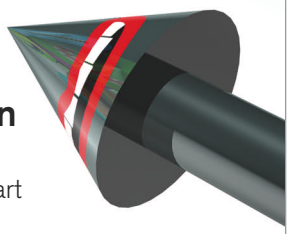
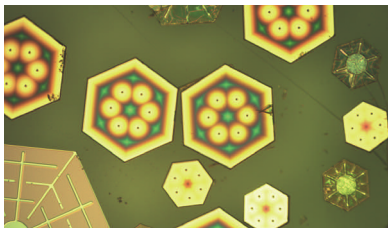


## Integration in the other direction



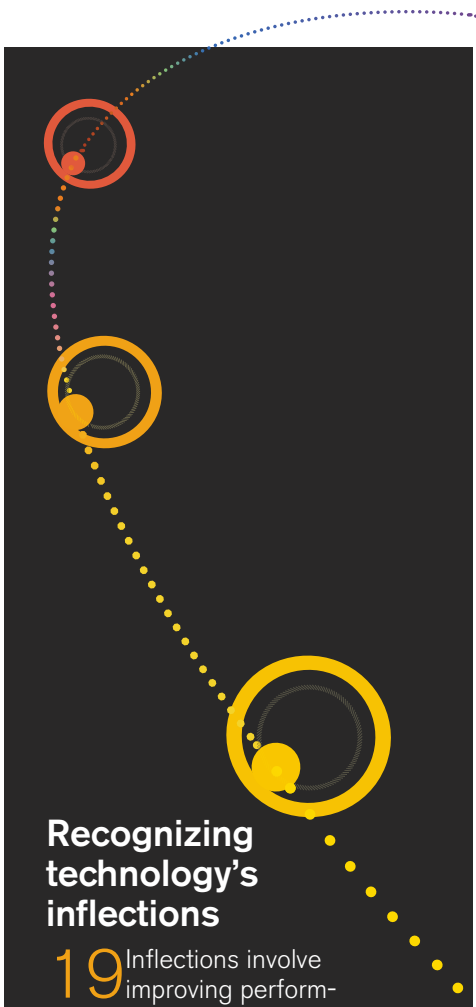
## pulse







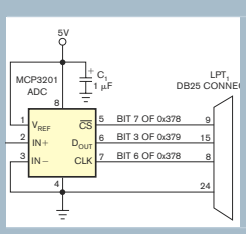




## Recognizing technology's inflections



# DESIGNIDEAS



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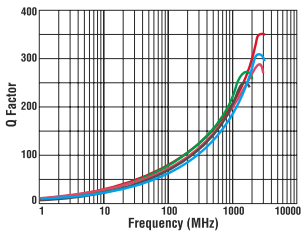


*Q factors are 3X higher than standard chip inductors*

And with their extremely low DCR, they can handle 4 to 8 times more current: up to 4.4 Arms.

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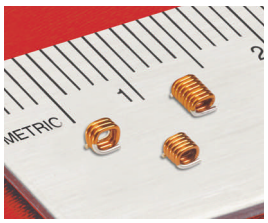
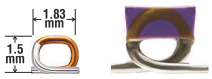



These coils are significantly smaller than existing air core inductors. We reduced the footprint by using close-wound construction and keeping the leads close to the body. The square shape cuts the height to as low as 1.5 mm and creates flat top and bottom surfaces for easy automated handling and stable mounting.

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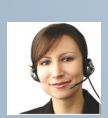

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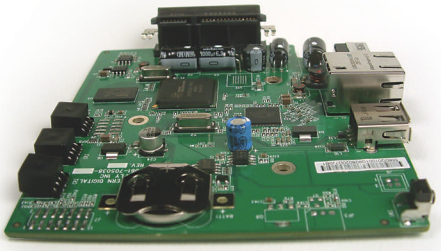

16


40

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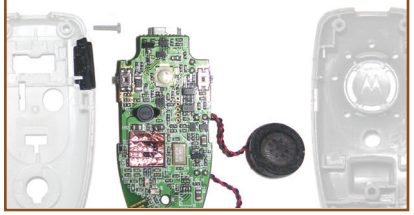


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BY RON WILSON, EXECUTIVE EDITOR

# IP networks' spread brings challenges to networking SOCs

Perhaps the most pervasive trend in networking today is the seemingly complete victory of IP (Internet Protocol) over rival protocols and the concomitant spread of GbE (gigabit Ethernet). GbE is replacing other alternatives and even packetizing legacy data flows and carrying them as encapsulated IP traffic. Along with carrying the traffic, the new fast networks also must provide the application-specific services that older networks have evolved. This trend is drawing together disparate networks into a single medium, vastly simplifying facilities management for network operators but creating a pain for silicon designers.

The highest-profile example may be in data centers, in which a 10-Gbit Ethernet fabric is drawing in three physical networks: InfiniBand for clustering, Ethernet for data, and Fibre Channel for storage. The convergence means that the single network must offer all the management and QOS (quality-of-service) features that three kinds of networks formerly provided. That scenario, in turn, has implications for network-adapter cards, classifiers, and fabrics throughout the network.

The same process seems to be uniting the various networks that serve users of the Internet. In the past, local networks for end users, the aggregation networks, fiber-access networks, and mobile backhaul networks all had distinct requirements. According to at least two semiconductor vendors, however, all of these networks may be converging. "We are seeing a need for a common feature set at several different layers of the network," says Jim McKeon, senior manager of product marketing for the service-provider segment at Broadcom. The need for features, including MPLS (multiprotocol label switching) and time synchronization, is cropping up across access, backhaul, and aggregation networks, he adds. Switches throughout the network essentially must support carrier-class services.

**Requiring all these functions becomes a serious challenge for SOC designers.**

Requiring all these functions across such a range of price and performance becomes a serious challenge for SOC (system-on-chip) designers. The high-end switches may require dedicated hardware and substantial memory to meet the demands of, for example, MPLS at wire speed. Yet low-end switches go into cost-sensitive markets and can't carry a silicon overhead for performance they don't need.

Fortunately for chip designers, a pattern still exists where functions occur in the network, according to Eric Hayes, Broadcom's senior director of product marketing. "At the edge, policy is user-based and generally oriented toward security concerns," he says. "As you move nearer the core, policy becomes more QOS-oriented. So while we have a uniform programming model across the families, the ability to apply policy varies from chip to chip."

Switch-fabric vendors aren't the only ones to see a growing commonality across applications. NPU (network-processing-unit) vendor Xelerated has been successfully serving the mobile backhaul market but finds fiber-access applications increasingly attractive, says Thomas Eklund, Xelerated's vice president of marketing and business development. Both markets face similar QOS issues but from different sources.

In the backhaul market, ATM (asynchronous-transfer-mode) networks often handle latency-intolerant time-domain-multiplexed voice traffic. In that market, the challenge is how to handle the increased data services that smartphones demand and that LTE (long-term evolution) promises. In fiber-access networks, built for sporadic and latency-insensitive Web browsing, the problem is IPTV. Both applications now seem to be converging on similar needs for management and QOS, and those needs look a lot like carrier-Ethernet specifications.

A parallel between the two convergences exists in data centers and in the global network, which, in the long run, may foretell an evolution to an architecture that distributes computing and storage resources throughout one network. In the meantime, SOC designers will be busy enough figuring out how to assemble and lay out the optimum family to spread a new level of classification and routing services across a lot of legacy applications. EDN

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INNOVATIONS & INNOVATORS

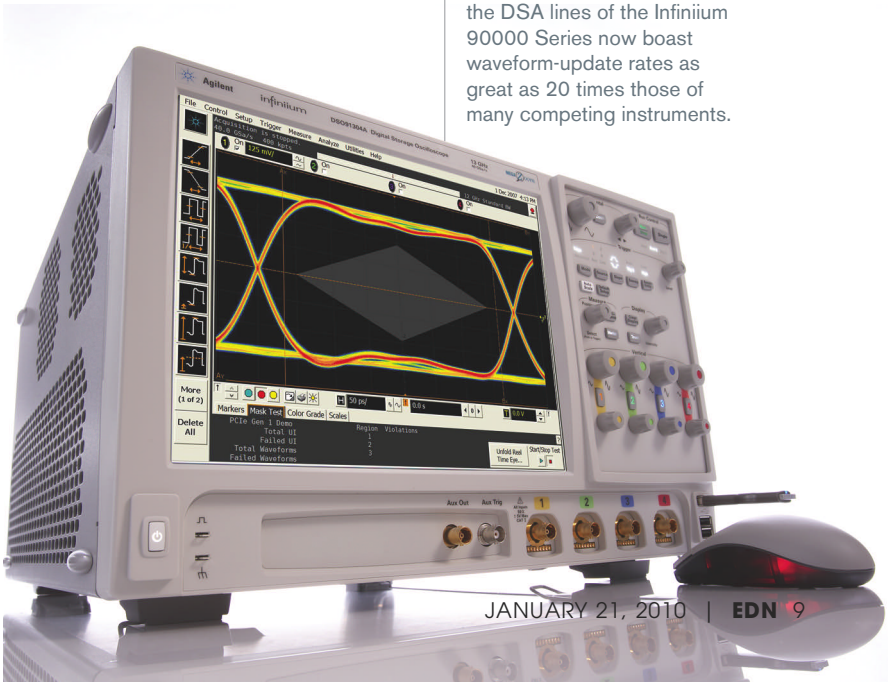
## High-performance scopes provide 20-times boost in waveform-update rates

Agilent Technologies recently announced the inclusion of faster PC hardware in its Infiniium 90000 Series oscilloscope family. With waveform-update rates more than 20 times those of many comparable scopes, these real-time instruments are the most responsive in their class, says the manufacturer. If you design high-speed serial data links, such as USB (Universal Serial Bus), SATA (serial advanced-technology attachment), or PCIe (Peripheral Component Interconnect Express), you rely on high-performance oscilloscopes to measure jitter and other signal parameters. Complex analysis is often critical but can be time-consuming. For example, using 20 million points of memory, competitive scopes can take more than 30 sec to run a jitter-separation algorithm. With their new performance enhancements, the Infiniium 90000 Series units yield results in less than 2 sec. This performance, combined with the scopes' optional industry-leading 1 billion points of memory, enables developers to quickly document their design performance across a wider range of test conditions.

Oscilloscopes also require processing power to remain responsive when manipulating complex algorithms, such as those for de-embedding the effects of stray and other circuit elements, such as probes and fixtures, which you cannot physically remove from the unit under test. The new scopes' improved responsiveness allows them to account for these effects without noticeably slowing the display of acquired waveforms. For example, the company's N5465A InfiniiSim waveform-transformation software takes advantage of the hardware acceleration to enable faster waveform updates in measurements that use de-embedding.

The performance enhancements are now standard at no additional cost on all Infiniium 90000 Series scopes. The 90000 Series includes two lines, DSOs (digital storage oscilloscopes) and DSAs (digital signal analyzers), each of which comprises six models that offer bandwidths of 2.5, 4, 6, 8, 12, and 13 GHz. Of these, the 8-, 12-, and 13-GHz models acquire a maximum of 40G samples/sec, and the 2.5-, 4-, and 6-GHz models acquire a maximum of 20G samples/sec. Base US prices for the DSO line range from $37,344 to $109,201; those for the DSA line range from $45,518 to $122,287. In addition to the features of DSO models with 20M samples of memory, DSA models add EZjit+ jitter-analysis software, serial-data-analysis software, and noise-reduction capabilities.**–by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/90000A.




Thanks to faster processing hardware, high-performance, 2.5- to 13-GHz-bandwidth scopes in both the DSO and the DSA lines of the Infiniium 90000 Series now boast waveform-update rates as great as 20 times those of many competing instruments.

### FEEDBACK LOOP

**"Holy smoke! Pun intended. Great story with a problem that I could certainly see myself falling into. A pat on the back for finding the solution with a solid bit of technical detective work."**

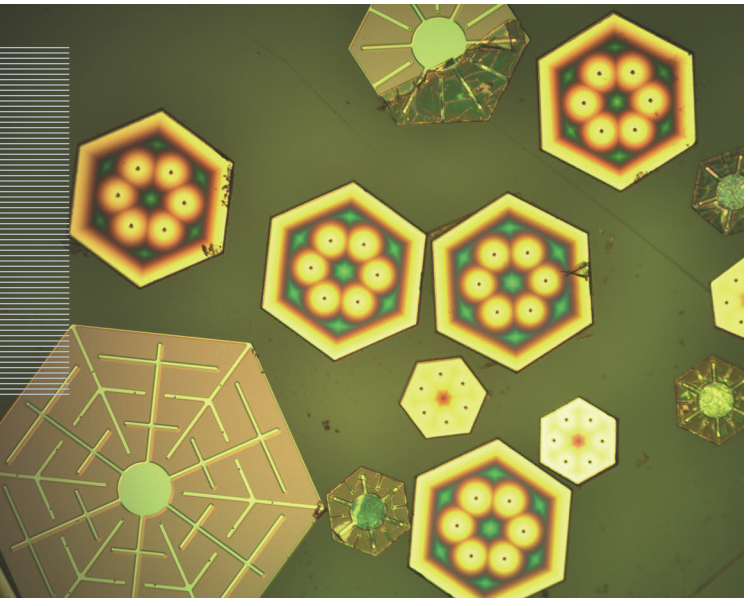
—Electronics-design consultant Bob Groh, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6711875. Add your comments.

# Tiny PV cells offer big benefits

Scientists from Sandia National Laboratories have developed tiny PV (photovoltaic) cells that are 10 times thinner than yet perform at about the same efficiency as conventional 6×6-in., brick-sized cells. The scientists believe that the PV cells offer potential applications that range from satellites to remote sensing and possibly to solar-energy-collecting clothing.

The crystalline-silicon, 14- to 20-micron-thick cells are much narrower than a human hair, which measures approximately 70 microns thick. The researchers used MEMS (microelectromechanical-system) techniques in the cells' fabrication and expect them to eventually be less expensive and have greater efficiencies than current PV collectors that employ 6-in.$^2$ solar wafers.

"Eventually, units could be mass-produced and wrapped around unusual shapes for building-integrated solar, tents, and maybe even clothing," says Greg Nielson, Sandia's lead investigator. The technology would enable hunters, hikers, or military personnel in the field to recharge batteries for phones, cameras, and other electronic devices as they walk or rest.



These crystalline-silicon, 14- to 20-micron-thick PV cells are much narrower than a human hair, which measures approximately 70 microns thick (courtesy Murat Okandan, Sandia National Labs).

> The change to small cells should be relatively straightforward.

Such microengineered panels could have imprinted circuits that would help perform other functions typically left to large-scale construction techniques and their attendant need for field-construction design and permits. "Photovoltaic modules made from these microsized cells for the rooftops of homes and warehouses could have intelligent controls, inverters, and even storage built in at the chip level," says Vipin Gupta, a Sandia field engineer. The technique would significantly reduce manufacturing and installation costs compared with current PV techniques, according to Murat Okandan, a Sandia researcher.

Part of the potential cost reduction comes about because the microcells require relatively little material to form well-controlled and highly efficient devices. According to Okandan, the cells use 100 times less silicon than conventional cells to generate the same amount of electricity. "Since they are much smaller and have fewer mechanical deformations for a given environment than the conventional cells, they may also be more reliable over the long term," he says. Because the cells are only hundreds of microns in diameter, manufacturers can fabricate them from commercial wafers of any size, including 300- and 450-mm wafers.

A commercial move to microscale PV cells would be a dramatic change from conventional silicon PV modules comprising arrays of 6-in.$^2$ cells. However, by using the same techniques that the MEMS, electronics, and LED industries use, the change to small cells should be relatively straightforward. The researchers formed each cell on silicon wafers, etched them, and then released them in hexagonal shapes, with prefabricated electrical contacts on each piece.

The Sandia-created cells can harvest electricity with 14.9% efficiency compared with off-the-shelf commercial modules, for which efficiency ranges from 13 to 20%. You can place solar concentrators over each cell to increase the number of photons arriving for conversion into electrons. The small cells allow the fabrication of cheaper and more efficient short-focal-length microlens arrays. The modules can directly output high voltages because of the large number of cells in the array. This feature should reduce wiring costs because of reduced resistive losses at higher voltages.

**–by Suzanne Deffree**

▷**Sandia National Laboratories**, www.sandia.gov.

## DILBERT By Scott Adams

# Energy harvester targets piezoelectric transducers

Linear Technology recently introduce the LTC3588-1 energy harvester, targeting low-energy sources, including piezoelectric transducers. The LTC3588-1 integrates a low-loss, full-wave bridge rectifier with a high-efficiency buck converter to harvest ambient vibrational energy through piezoelectric transducers and then convert it to a well-regulated output to power application microcontrollers, sensors, data converters, and wireless transmission components.

The LTC3588-1 operates from an input-voltage range of 2.7 to 20V, making it suitable for a wide array of piezoelectric transducers, as well other high-output-impedance energy sources. Its buck dc/dc converter delivers as much as 100 mA of continuous output current or even higher pulsed loads. You can program its output to one of four fixed voltages of 1.8, 2.5, 3.3, or 3.6V to power a wireless transmitter or sensor. Quiescent current is 950 nA with the output in regulation at no load, maximizing overall efficiency.

The LTC3588-1 interfaces directly with a piezoelectric or alternative ac-power source, rectifies a voltage waveform, stores harvested energy in an external storage capacitor, and dissipates any excess power through an internal shunt regulator. A quiescent current of 450 nA and an undervoltage-lockout mode with a wide hysteresis window enable charge to accumulate on the storage capacitor until the buck converter can efficiently transfer a portion of the stored charge to the output. In its no-load sleep state, the LTC3588-1 regulates the output voltage, consuming only 950 nA of quiescent current while continuously charging the storage capacitor. The LTC3588-1 requires minimal external components and comes in a 3×3-mm DFN or a thermally enhanced MSOP-10 package.

The LTC3588-1 operates from an input-voltage range of 2.7 to 20V, making it suitable for piezoelectric transducers and other high-output-impedance energy sources.

The LTC3588EDD-1 is available in a 3×3-mm DFN package, and the LTC3588EMSE-1 is available in a thermally enhanced MSOP-10 package. Prices start at $2.95 (1000). Industrial-temperature-grade versions, the LTC3588IDD-1 and LTC3588IMSE-1, are also available, with prices starting at $3.47 (1000).

**–by Fran Granville**

▷**Linear Technology Corp**, www.linear.com.

01.21.10

## CADENCE VIRTUOSO RELEASE HIGHLIGHTS USABILITY

**A new release of Cadence's Virtuoso custom-design platform is about usability, not about solving new classes of technical-design problems. You could take this as a sign that design teams are not developing radically new IP (intellectual property) or hurrying to new process nodes and hence aren't facing new technical challenges. Alternatively, you could conclude that, struggling with constrained budgets, Cadence customers want to see fewer engineer-hours going into necessary tasks, even if the results stay the same. Both conclusions seem consistent with design trends in the new global reality.**

**The usability features Cadence selected relate mostly to the user-hours issue. For example, 6.1.4 includes enhanced ability to use an interactive graphics interface for design entry and editing. The release brings space-based wire-placement technology–from Cadence's space-based router batch tool–to the Virtuoso wire editor, potentially eliminating the need for iterations in the interconnect-design process. The company has also improved the way Virtuoso inputs and handles design constraints. It now includes a wizard for entering constraints, as well as new tools for managing the constraints, back-annotating to them during the design process, and verifying that the layout team meets the constraints.**

**Another significant aspect of the release is its metrics-driven productivity initiative, which addresses user-interface efficiency. This program will have a top manager assigned to it, will get resources, and will influence the way Cadence addresses its market. In the case of the 6.1.4 release, the initiative means that Cadence retrieves log files from user sessions–making sure that the users are informed and consenting–and builds from the files a database of user effort with such functions as mouse clicks and mouse motions. Cadence has built an internal data-mining widget to explore this data, looking for patterns of high user-interface traffic, and is using the results to streamline tasks that seem to require a lot of thrashing about.**

**The results of this analysis are often surprising, according to John Stabenow, Cadence's group director of marketing. For example, analysis shows that the simple ruler function in the layout user interface was both heavily used and inefficient. The Cadence team used this information to come up with an intelligent ruler function in the new release, which Stabenow says cuts 90% of the zooms and clicks necessary for dimension measurements.–by Ron Wilson**

▶**Cadence Design Systems, www.cadence.com.**

# Solid-state-drive counterattack packs a two-part punch

What does Seagate, the largest hard-disk-drive manufacturer, do when it's late for the inevitable transition from hard disks to solid-state drives? The company recently revealed its strategy for answering that question, announcing a two-part plan. Seagate unveiled 160- and 250-Gbyte hard-disk drives, the first two members of its 7-mm-wide, 2.5-in. Momentus Slim family, and released Pulsar, its first product offering in the solid-state-drive category.

The Momentus Slim drives feature 8-Mbyte RAM buffers, 3-Gbps SATA (serial-advanced-technology-attachment) system interfaces, and 5400-rpm rotational speeds. The company provides no architectural or pricing details, although the devices are most likely single-platter designs. With the units, Seagate is competing with 1.8-in. hard-disk drives from competitors such as Samsung (www.samsung.com) and Toshiba (www.toshiba.com), 2.5-in. hard drives from all suppliers, and flash-memory-based mass storage in various form factors.

Seagate's Momentus Slim (top and center) is thinner than a conventional 9.5-mm hard drive. Pulsar (bottom) represents the company's first foray into the solid-state-drive market.

Although Momentus Slim is thinner than a conventional 9.5-mm hard-disk drive and even thinner than some three-platter, 12.5-mm configurations, it does not enjoy guaranteed market success because it is currently a sole-sourced product and because it's a rotating magnetic hard—albeit one that delivers attractive capacity and dollar-per-gigabyte metrics. It thus burns a notable amount of power and has reliability challenges.

Meanwhile, Seagate is shipping Pulsar to customers for qualification. The company based Pulsar on SLC (single-level-cell) flash-memory technology, thereby delivering faster writes than MLC (multilevel-cell) alternatives—at a dollar-per-gigabyte trade-off—and aimed at enterprise applications.**–by Brian Dipert**

▷**Seagate**, www.seagate.com.

## PROCESSOR PUSHES POWER EVEN LOWER

**Silicon Labs' 25-MHz C8051F91x/0x microcontrollers sport active-mode current consumption of 4 mA, or 160 µA/MHz, at full speed and 1.8 or 3.3V operation. They also support a sleep mode with a current draw as low as 10 nA while maintaining full RAM retention. The current draw is 300 nA with an active real-time clock and brownout detection. This level of power consumption allows these microcontrollers to target smart meters, RFID tags, personal medical devices, sensor interfaces, energy harvesting, home-security systems, and smoke- and fire-detector designs. The F91x/0x devices can fully wake up from sleep in less than 2 µsec.**

**The devices support 8- and 16-kbyte flash-memory options as well as a 12-bit ADC that includes an autonomous power-saving burst mode with a 16-bit automatic averaging accumulator that allows sampling without waking up the processor core. An integrated dc/dc converter supports operation to as low as 0.9V to enable operation with AA or AAA batteries, and all of the on-chip peripherals and flash are fully operational down to 0.9V. The dc/dc converter can supply 65 mW of output power to drive LEDs, RF transceivers, and sensors.**

**Software-development support for the F91x/0x family includes the C8051F912 development kit, F912-based ToolStick, and optional ToolStick programming adapters. The company provides sample code for the C8051F9xx and a battery-life estimator to help designers optimize power. Silicon Labs offers an RF-to-USB (Universal Serial Bus) reference design to demonstrate subgigahertz wireless and USB operation. The C8051F91x/0x family is available now in a 24-pin, 4×4-mm package for prices starting at $1.53 (10,000). The C8051F912 development kits are available for $99. The ToolStick912DC daughtercard sells for $9.90, and the ToolStick912 programmer costs $69.–by Robert Cravotta**

▶**Silicon Laboratories, www.silabs.com.**

01.21.10

# VOICES

## iFixit's Kyle Wiens: extending electronics' life span

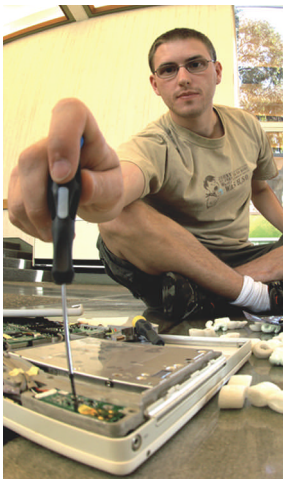
Kyle Wiens is the co-founder and chief executive officer of iFixit, a parts retailer for the iMac, iPhone, iPod, and similar products. The company is often the first to publish teardowns—inside glances into the electronics—of Apple products. From its origins in a dorm room at California State Polytechnic Institute—San Luis Obispo in 2003, iFixit has morphed into a collaborative repair community for electronic consumer goods that might otherwise end up in a landfill after a few years of use. Along the way, Wiens developed an understanding of the cradle-to-grave life cycle of an electronic product, including the environmental cost of e-waste—electronics that end up in the trash—as well as an appreciation for how people salvage, repair, and reuse electronics in developing countries.

**How did you become aware of the implications of the cradle-to-grave life cycle of electronics?**

A We got our start selling parts for iBooks, and the only way to get replacement parts was to buy old iBooks off eBay and scavenge them for parts. It's not usually worth our time to work on PC knockoffs, but Mac laptops are about the most expensive computers out there. Then, this summer, I went to Africa and spent three months researching what happens to our e-waste. For example, CRT displays are virtually obsolete here [in the United States], but in Africa they can have another life. Scavengers salvage CRTs from landfills that still work but have yellowed cases. They paint them white and sell them. The problem is with the stuff that's marginally working or is dead. That's where they have a challenging time because they're working through large volumes of stuff, and, if it isn't immediately clear how to fix it, it's not necessarily worth their time to figure it out. They're hoping to make maybe $5 a day, which they can reasonably do working on CRT displays.

**Why did you go to Africa?**

A I'm trying to show people how people fix things in developing countries. You get a power supply that's not functional; where do they get information on how electronics work? One way is to "hyperspecialize." One person works on power supplies while another one works on a type of cell-phone logic board, repairing traces on cell-phone boards when the physical board itself is cracked. It's pretty impressive. They don't do things the "right" way—ever. They use brute force; they get things done. But once they get something figured out, then that's their niche in the community. That's the same anywhere: You find something



that you're good at, and you focus on it. There's a Swahili term for it—*jua kali* [literally, "hot sun"]—and the closest I can come to it is our term "hackers."

I went to one six-story building in downtown Nairobi [Kenya] that was full of electronics-repair businesses, some doing specialized repair and some reselling CRTs and TVs. Out of chaos emerges some organization, with people clawing a niche for themselves.

**What can we in the United States do to move the world away from throwaway electronics?**

A We need to try to push the electronics green standards to include reliability. Even the environmentally friendly ROHS [reduction of hazardous substances], which is causing a switch away from lead-based solder, dramatically reduces the reliability of electronics. Look at the military: It requires lead-based solder because it understands the reliability problems. When [iFixit is] working on boards with non-lead-based solder, the job is four times more difficult. I'm not sure that switching away from lead solder is the most environmentally friendly thing to do in the long run.

**What should engineers keep in mind to minimize e-waste when designing products?**

A The number one thing is to not build products with consumables like lithium batteries that are not user-replaceable. A lithium battery has only 200 cycles; you can't in good conscience not allow the user to replace it. For example, Apple has a nonreplaceable battery in the iPhone, which I think is the wrong decision. Motorola has made the Droid [cell phone] so that you can replace the battery and has made it a selling point.

Designing a product for future expansion is also important, such as using a MicroSD card instead of built-in flash memory. I should not have to throw away my iPhone and get a new one to upgrade from 8 to 16 Gbytes. I'm sympathetic with people who want to get the new iPod Nano this year, but what happens to the old one? So it's not cool enough for you, but … as long as it still works, someone should be able to use it.

I visited a recycling place in South Africa where they get the same machine coming through their place four to five times. Every few years, the machine would come back as the owner upgraded, and the recycler would sell it back to someone farther out in the country. If you've just gotten electricity out in a village and you run a little dry-goods shop, being able to run VisiCalc on an Apple II can change your life. We [in the United States] have forgotten the magic of how powerful the technology that we had 10 years ago was and how it can revolutionize life.

**–interview conducted and edited by Margery Conner**

BY BONNIE BAKER

# Jitter and the ins and outs of SNR

When you use a high-speed ADC, you expect the performance to meet the published data-sheet SNR (signal-to-noise-ratio) value. When you test the ADC's SNR, you might attach a low-jitter clock device to the converter's clock pin and apply a reasonably low-noise input signal. Several sources of noise errors can cause your converter to fail to meet the publisher specs.

If you are certain that you have a low-noise input signal and a good layout, the combination of the input-signal frequency and the jitter from your clock device is probably the cause of the problem. You will find that low-jitter clock devices are adequate for most ADC applications. However, if both the input-signal frequency to the ADC and the converter's SNR are high, you may need to improve your clock circuit.

Low-jitter clock devices, at best, have advertised 1-psec jitter specifications, or you can generate an equally inferior clock signal from an FPGA. Issues that contribute to the SNR error of your high-speed ADC include ADC quantization noise, DNL (differential-nonlinearity) effects, the converter's effective internal input noise, and jitter. You can determine whether jitter is the problem by using the following **equation**, which provides the ADC's SNR error that the external clock and ADC jitter exclusively generate: $SNR_{CLK} = -20\log_{10}(2\pi f_{IN} \times t_{JITTER\text{-}TOTAL})$, where $f_{IN}$ is the input signal's frequency to the converter and $t_{JITTER\text{-}TOTAL}$ is the rms jitter from the clock signal and ADC clock's input circuitry. Note that $f_{IN}$ is not the clock frequency ($f_{CLK}$). A jitter of 1 psec from the external clock to the ADC is adequate for some but not all high-speed ADC applications (**Figure 1**).

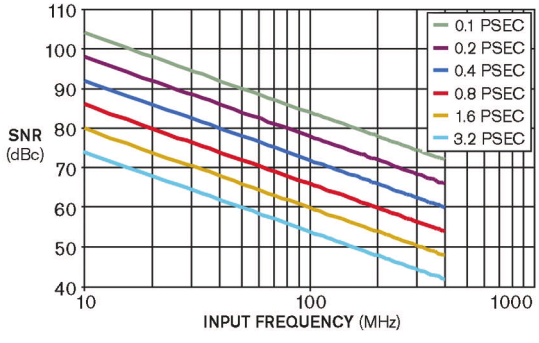



Figure 1 The SNR due to jitter is a function of the input signal's frequency.

The **equation** allows you to calculate an estimate of the required clock jitter for a given ADC. For instance, with an ADC with a specified 70-dB SNR and a 100-MHz input signal, you can calculate the value of $t_{JITTER\text{-}TOTAL}$ as 503 fsec. If the input ADC's aperture jitter is 150 fsec, you can make a high estimate of the external clock-jitter requirements with the following **equation**: $t_{JITTER\text{-}CLK} = \sqrt{(t_{JITTER\text{-}TOTAL})^2 - (t_{JITTER\text{-}ADC})^2}$, where $t_{JITTER\text{-}CLK}$ is the jitter that the clock injects into the ADC and $t_{JITTER\text{-}ADC}$ is the ADC's aperture jitter, clock amplitude, and slope. Continuing with the estimate, make $t_{JITTER\text{-}ADC}$ equal only to the ADC's internal jitter of 150 fsec and ignore the effects of the clock amplitude and slope. Using this **equation**, a high estimate of $t_{JITTER\text{-}CLK}$ is 480 fsec.

This column only scratches the surface of the issues behind perfecting the clock signal to a high-speed ADC. You need to give further attention to the clock amplitude and slope because they affect the system jitter. Additionally, you must understand how to implement the hardware portion of a low-jitter clock circuit.

For your next clock design, remember that clock jitter affects the ADC's SNR performance in input frequency to the ADC and the actual clock jitter. Additionally, be skeptical of clock-device vendors' claims. Use the evaluation board from the ADC vendor to test your clock sources before you develop your product. You will be happier with the end results. EDN

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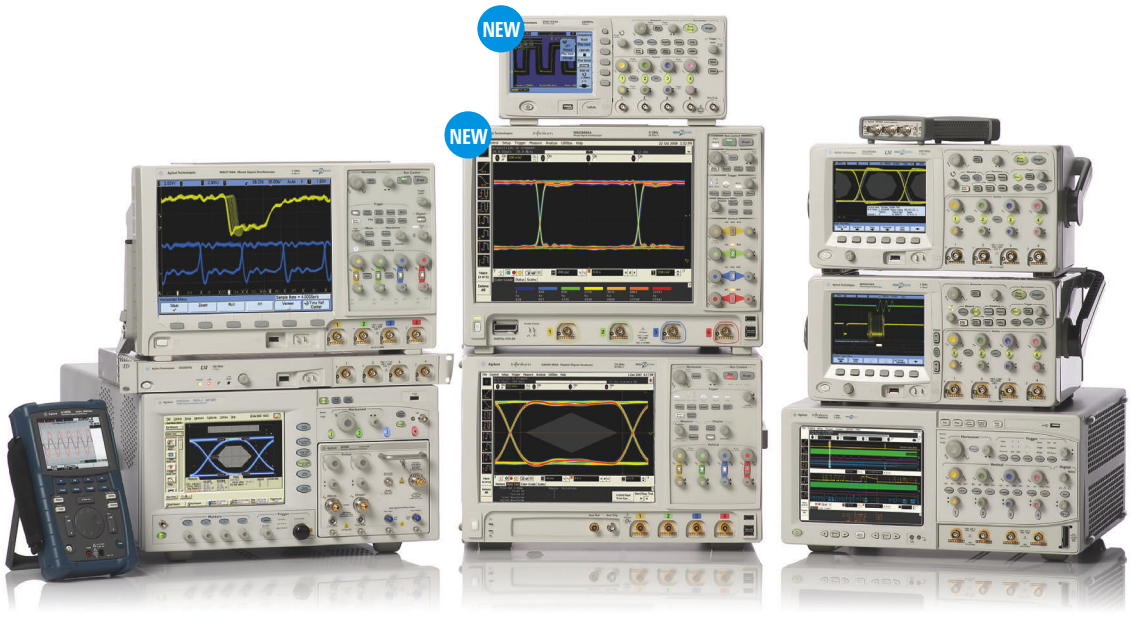


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# Analyzing a NAS

Make it better, but make it cheaper, too. This seeming contradiction confronts consumer-electronics engineers designing each new generation's worth of hardware in comparison with its predecessor. How did Western Digital address the disparity? And how far has single-drive consumer NAS (network-attached-storage) technology progressed in the past few years? (See "Mini-NAS: an unfinished masterpiece?" *EDN*, Oct 26, 2006, pg 40, www.edn.com/article/CA6382651.)

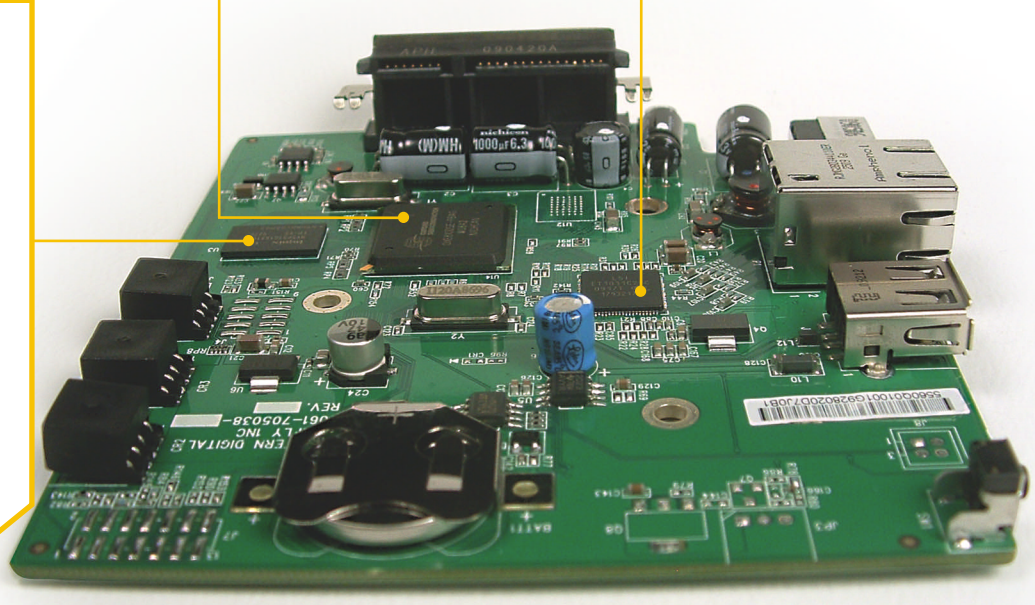
Western Digital's My Book World Edition NAS device is so named because users can potentially access it from anywhere in the world. Befitting its front-panel illumination scheme, the second-generation iteration is commonly known as the "white-light" model, which follows the initial "blue-ring" version from two years before. This highly integrated design includes only a few chips. The backside (not shown) of the PCB (printed-circuit board) is virtually bare.

The air-cooling vents arrange in Morse Code patterns that spell out words such as "personal," "reliable," "innovative," "simple," and "design." The My Book World Edition includes a USB (Universal Serial Bus) port, but the factory-supplied firmware enables its use only to augment the NAS' internal memory, not as a print-server portal.

The heart of the My Book World Edition is Oxford Semiconductor's OXE810 SOC (system on chip), now known as the PLX810 because PLX Technology acquired the company a year ago. This SE version of the IC supports single-drive configurations; Western Digital's My Book World Edition II contains the PLX810DSE, which handles two hard-disk drives and optionally implements RAID (redundant-array-of-inexpensive-disk) 0 and RAID 1 drive configurations.

You waste intra-NAS performance if the network connection is the speed bottleneck. The PLX800 integrated only a 10/100-Mbps Ethernet PHY (physical) layer, so Western Digital bolted an external 1-GbE (gigabit-Ethernet) transceiver to the SOC's PCI (peripheral-component-interconnect) port. The PLX810 integrates 1-GbE MAC (media-access-controller) capabilities. LSI Logic's ET1011C2-C 1-GbE PHY completes the Ethernet picture.

The PLX810 contains an ARM9 core running at 367 MHz versus 200 MHz on the PLX800 used in the first-generation My Book World Edition NAS. The PLX810 also mates to 1 Gbit of DDR2 SDRAM with a 16-bit interface, whereas the PLX800 used DDR SRAM. The end results of these SOC enhancements are claimed 39-Mbyte/sec read and 25-Mbyte/sec write speeds, versus 7.5-Mbyte/sec reads and writes on the PLX800.



RAQ's

# Rarely Asked Questions

Strange stories from the call logs of Analog Devices

## VFB or CFB that is the question!

**Q.** Why is it, that voltage feedback amplifiers seem to dominant the op amp landscape compared to current feedback amplifiers?

**A.** Some may argue when it comes to selecting an op amp, it's more of a personal preference or taste in amplifiers. As in life we tend to choose things (op amps included) based on personal experience. That is probably why quite often engineers select voltage feedback (VFB) op amps over current feedback (CFB) op amps.

So why is that? Well I'm sure that there are lots of reasons, just the sheer numbers, there are a lot more VFB amplifiers than CFB to chose from, but another reason is education. In colleges most often voltage feedback is the standard that is taught in the classroom. Many of the op amp examples found in text books, labs or simulations focus on VFB. You'll find very few examples of CFB op amps described in college text books, and if you do, they will only be briefly mentioned.

Now we can't possibly cover all the differences and options between current feedback and voltage feedback amplifiers here, but we can discuss a few key points. First the design equations used for voltage feedback amps work equally well for current feedback amps, so nothing new to learn there. Voltage feedback amplifiers have a fixed gain bandwidth product; current feedback amplifiers do not, so you can have high gain and high bandwidth with a CFB amp. Voltage feedback amps have two high input impedance nodes, current feedback amps only have one, the non-inverting input; the inverting input is a low impedance input. Voltage


feedback amplifiers have "open loop gain"; current feedback amps have "open loop transimpedance." Current feedback amplfieirs have very wide bandwidths and very high slew rates compared to VFB amps. The feedback resistor plays a large role in CFB amplifier stability, unlike voltage feedback amplifiers. This limits the choices of feedback resistor (the value can be found in the manufacturer's datasheet) it can also limit the value of the gain set resistor.

We've only scratched the surface here, regarding current and voltage feedback amplifiers. Current feedback amplifiers provide engineers with another powerful option when designing circuits. We have a great deal of additional information on current feedback and voltage feedback amplifiers which can be accessed by clicking on the link below. So next time you're in the mood for a voltage feedback amp, take a moment and look the menu over, you may find a tasty alternative awaits you.

**To Learn More About Voltage Feedback and Current Feedback Amplifiers**
http://designnews.hotims.com/27735-101

**Contributing Writer John Ardizzoni is a Senior Application Engineer at Analog Devices in the High Speed Linear group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 29 years experience in the electronics industry.**

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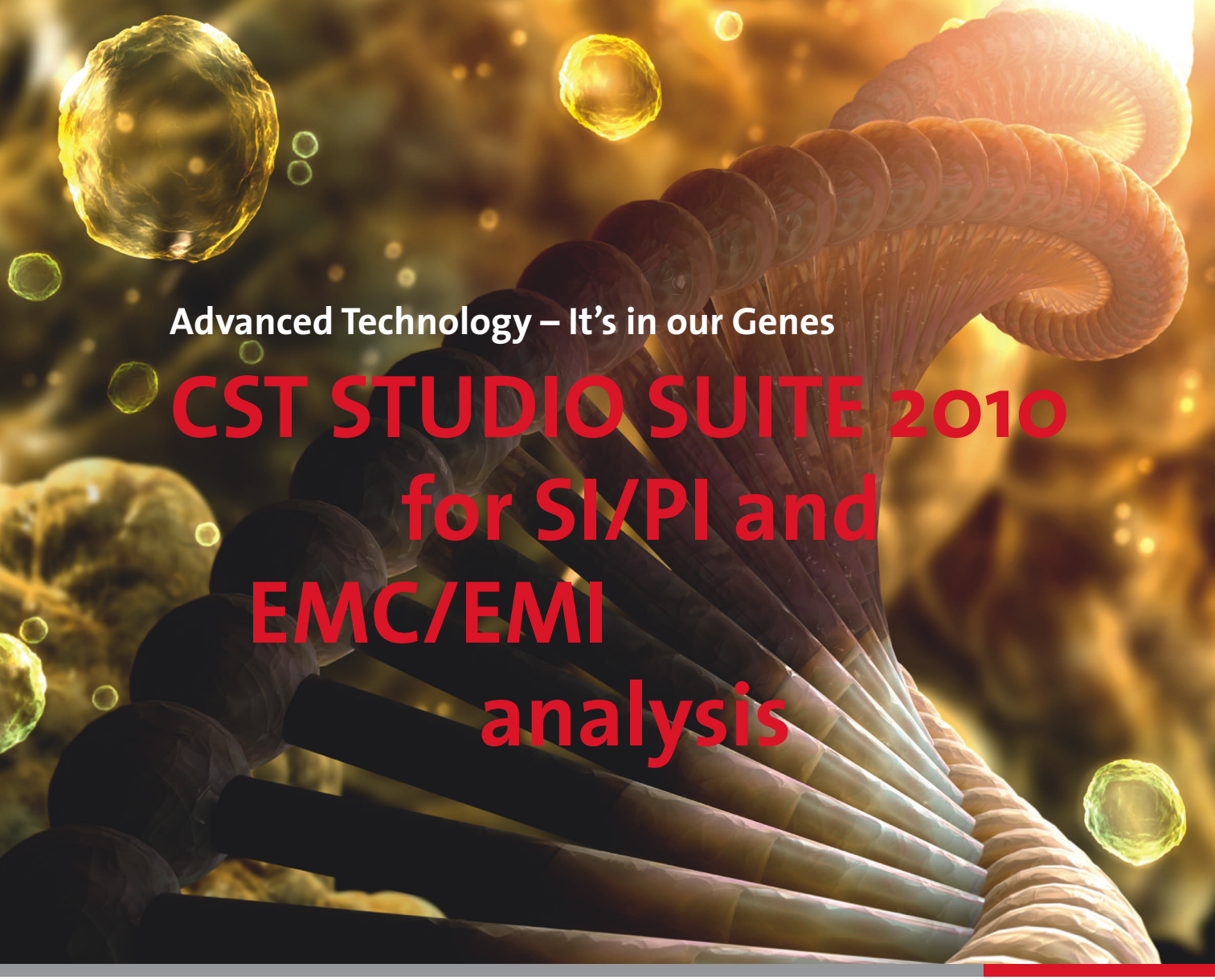

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CHANGING THE STANDARDS

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

# RECOGNIZING TECHNOLOGY'S INFLECTIONS

INFLECTIONS INVOLVE IMPROVING PERFORMANCE, COST, OR BOTH.

MORE IMPORTANT, THEY SIMPLIFY SYSTEMS FOR THEIR USERS.

Technology inflection points occur when there is a fundamental change in how technology achieves some goal or how you use that technology. These changes can profoundly affect entire industries, but inflection points are sometimes not apparent when they are occurring. A company's ability to recognize and respond to these inflection points can mean the difference between becoming a huge winner and turning out as a historical footnote. Technology inflection points for embedded processing have the added complexity of being mostly invisible to end users, so the populace for the most part doesn't notice fundamental shifts.

Consider, for example, Intel's 4004 microprocessor and Texas Instruments' 32010 DSP. The genesis of the Intel 4004 processor was the result of Nippon Calculating Machine Corp's contracting with Intel to convert Nippon's Busicom 141-PF printing-calculator logic design into 12 custom chips, of which Nippon sold approximately 100,000 units. The company was looking to take competitive advantage of the availability of MOS LSI (large-scale-integration) technology to shift from electromechanical calculators to electronic ones. The Intel design team for the MCS-4 project proposed to substitute the 12-chip approach with a four-chip implementation that included a single chip that designers could program for use in multiple tasks. The programmable-chip approach made the system possible and provided a level of flexibility and reliability that the 12-chip approach could not. With a payment of $60,000, Intel was able to change the license agreement between the two companies so that Intel secured the rights for the microprocessor design and the rights to market it for applications other than calculators.

Intel in November 1971 introduced the 4004 microprocessor, the first general-purpose "building-block" processor on the market, and it has since been a leading player in the microprocessor market. The programmable microprocessor fundamentally changed how manufacturers designed and built products, replaced mechanical-control mechanisms with microcontrollers, and enabled more precise control and monitoring of all types of end systems.

In contrast, Texas Instruments in 1983 introduced the TMS32010 DSP—not the first on the market but the first to integrate a 16-bit MAC (multiply/accumulate)-unit accelerator that made it easier for developers to use multiplication in their applications. According to Ray Simar, a professor at Rice University and a former TI fellow and DSP-design-team manager, the company originally built and marketed the 32010 for speech processing but quickly discovered that its customers were using it for other applications. TI then changed its marketing position and message to general-purpose

digital signal processing and has since been a leader in that market. Digital signal processing has become so pervasive that you could consider it an embedded technology within embedded systems. In that scenario, semiconductor suppliers are now providing software stacks to allow access to the integrated application-specific accelerators without the need for developers to become signal-processing experts (**Reference 1**).

## HIDING COMPLEXITY

Inflection points are not just about technical capability; capability alone is usually not enough to cause an inflection point. The inflection shift involves hiding complexity from the user of the system. This approach does not reduce the overall complexity of the system but instead simplifies the learning curve and understanding model that a user must develop to effectively use the technology. Consider Microsoft's Windows operating system and Apple's iPhone products. Microsoft Windows did not encourage an inflection in the market until Version 3.0 emerged—five years after Version 1.0. Version 3.0 simplified the management of the vast array of optional peripherals available for the desktop PC, and it gained widespread third-party support. It also enabled, simplified, and hid much of the complexity of sharing data between programs. Desktop computers were already supporting a robust third-party-peripheral market, and Windows 3.0 hid some of the complexity so that more users could confidently choose best-in-class components. They could transfer data among applications, but that task involved the use of translation programs and the loss of data from special features. Windows 3 hid the complexity of selecting those translation programs and provided a data-interchange format and mechanism that further improved users' ability to share data among applications.

The Apple iPhone changed the way people think of touch and gesture interfaces, but it was not the first use of touch interfaces on a smartphone (**Reference 2**). The IBM Simon predates it by 14 years. The iPhone enjoys significantly higher processing performance than the earlier Simon device, however, allowing the iPhone to incorporate more smarts in the control system to successfully handle input ambiguities. The system does a better job than earlier systems of adapting to users.

### AT A GLANCE

- Technology inflections are easier to spot in hindsight, but correctly responding to the market during an inflection can produce large winners.
- Technology inflections happen when they integrate the right mix of components to simplify a developer's view of system complexity.
- As software consumes even more of a design budget, the hardware must support the tool's ability to abstract more of the system complexity.

However, it is still unclear whether this round of touch-sensitive and gesture-recognition systems, which the iPhone represents, is sufficient to enable an inflection point in embedded-system designs. In an attempt to avoid the lost opportunity that Nippon experienced with Busicom, many semiconductor companies are taking no chances. Last year, a dozen or so companies released or upgraded their touch-sensing kits. Although many touch-sensing kits are available, touch interfaces may not sufficiently simplify them to justify their use in embedded designs. A later article will explore these kits' maturity, level of abstraction, bundled software, and development tools.

The opportunities increase to "waste" transistors on features that make it easier, faster, and more reliable to build systems in fundamentally different ways.

## ADDING INTEGRATION

A technology inflection point involves a fundamental shift in how designers and users perform their tasks. The economical integration of formerly separate pieces enables this shift. The 4004 integrated a software-programmable core to replace a purely custom logic design. The TMS32010 integrated a 16-bit hardware accelerator and an accompanying instruction-set architecture that simplified the implementation of multiplication. Windows 3 integrated device drivers and data sharing to simplify the support of the available peripherals and applications. The iPhone integrated smarter input processing to enable the touch and gesture interface to reliably handle ambiguous conditions that plagued similar interfaces in earlier products.

The ability to recognize an imminent inflection point is not essential, but it lessens the reliance on luck to respond appropriately to the market reactions to such changes. You may wonder whether inflection points share some common trait that can help you identify when such an opportunity exists. As Moore's Law continues to approximately every two years double the number of transistors that you can inexpensively place on an IC, the opportunities increase to "waste" transistors on features that make it easier, faster, and more reliable to build systems in fundamentally different ways from before. You can use these extra transistors to make redundant resources and to provide resources for other parts of the design value chain, such as operating systems, development tools, and on-chip debugging and profiling resources.

Long before multicore processors became popular, processor architectures had evolved on a path toward having more parallel resources. The scale of the number and organization of transistors available to a processor architecture changes what is important to developers. The earliest transistor-count-constrained architectures often could not afford to waste any transistors on redundant resources. The transition to a register file made sense as more transistors became available to waste on parallel, redundant accumulators that would greatly improve processing performance because it could eliminate temporary data moves that were necessary when there was only one accumulator. This type of change provided the first level of relief for clock-cycle counting for many applications.

Transistors eventually became available for designers to waste on redundant, wider address and data buses and accompanying arithmetic units. Witness the ingenuity of 8-bit 8051 processors to deliver an address space exceed-

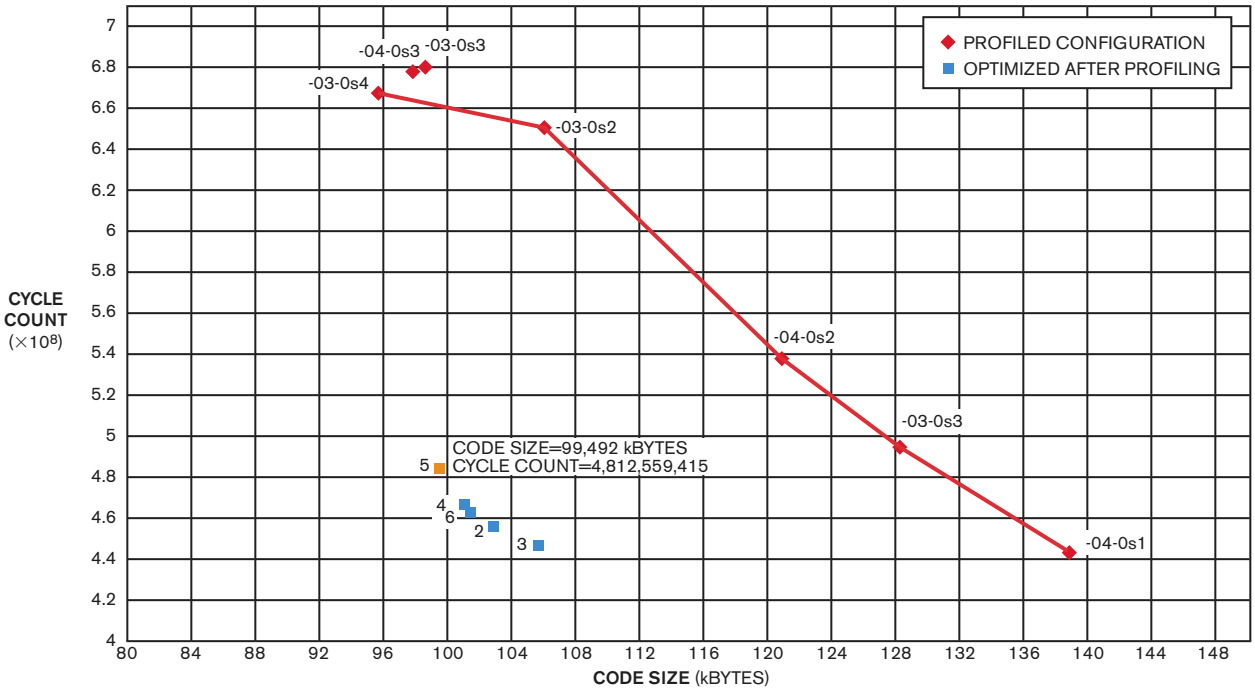


Figure 1 The Ceva compiler performs multiple compilations of each function with different settings and then presents the trade-offs.

ing 2 Mbytes through block addressing and bank switching. As designers could economically waste more transistors on larger, parallel, and redundant integrated memory structures, the processors could perform more complicated tasks because the software code could account for more details in the task it needed to perform. Processors with large-enough address spaces allow developers to avoid the complexities of managing bank switching and conceptually treat memory as one block. The expansion of the available memory helps relax the urgency of byte counting in many designs.

The ability to waste transistors on a parallel and redundant hardware multiplier accelerator opens a new industry for signal processing. The processor retains its ALU (arithmetic-logic unit) in addition to the new multiply accelerator, and designers can still use the ALU to perform multiplication—albeit more slowly. You can make similar statements for nearly every accelerator that contemporary processor architectures integrate.

The earliest integrated redundant resources hid or transferred some of the complexity away from the software developer, and each of these transfers enabled the processors to take on complexities that they could not previously handle. Processors with wide-enough ALUs or hardware accelerators allow developers to avoid having to break up multiplications, floating-point operations, Viterbi algorithms, and other tasks into lower- and higher-order bit operations that require manual management and combination. In contrast, general-purpose multicore implementations often require software developers to explicitly identify where parallelism exists—a step back to where the industry was.

Architectural inflection points do not necessarily apply across the entire application area. An innovation that transforms one application might be inappropriate for another. Pipelines and caches are redundant resources that can help reduce the complexity of managing memory-access times for software developers by masking the significant access latency when the system must access data in cheaper memory that is farther from the core (**Reference 3**). However, pipelines and caches are inappropriate for some embedded designs, especially those, such as motor controllers, that require fast, deterministic behavior. As a result, many motor controllers do not use pipelines or caches because they would unnecessarily increase the developer's exposure to complexity.

Steve Leibson, a consultant for semiconductor and EDA companies and a former editor-in-chief of *EDN*, points out that energy dissipation drives the need for many contemporary parallel-processing implementations and algorithms. It is no longer practical to keep driving clock rates faster because the industry has crossed a threshold in which static leakage current is a larger issue than it was at larger process geometries and slower clock rates. To deliver more processing performance for a unit of time, high-end processors employ multiple cores in one device. For parallel-processing applications, such as video processing, this approach works well for the same reasons that extra registers and accelerators work well for other applications: They offload some of the data management and scheduling complexity from the software developer.

However, similar to pipeline and caches for highly deterministic applications, applying a multicore approach to a general-purpose problem exposes and complicates the software developer's already-significant load. In addition to the proper execution of the functional tasks, the software developer must prevent timing dependencies that were simpler in a single-instruction-engine architecture. Another area of complexity is how to identify parallelism, partition, and balance the workload across

the cores. A memory architecture that you can no longer treat as a single block further complicates this design task; data may reside in main memory or in one or more of several local memories of other cores—each with different implications for access latency. The developer may have to provide data coherence in software if the processor lacks a hardware coherence controller. All of these complexities scream for software-development tools to help shoulder the additional load from the software developer.

## SOFTWARE TOOLS

Along with the processor-architecture changes, software-development tools have undergone a number of inflection shifts, but they happened in step with the changes in silicon. The earliest processors might come with an assembler and some application notes to help developers figure out how to use them. The assembler was a direct reflection of the underlying architecture and instruction set; it was primarily a tool to help the developer think in terms of the steps the processor executed. The developer had to manually translate even simple algebraic expressions into a series of machine reads, stores, shifts, and additions.

High-level languages helped simplify the translation to machine or assembly code, but they usually produced code that was significantly worse than what a developer could do manually—on a system with severely constrained resources. Processor architectures became more compiler-friendly as they implemented register files and orthogonal instruction sets and as they could support larger memories. In other words, fewer improvements in compiler technology would have occurred if the appropriate silicon support had been lacking. Contemporary compilers are good enough to use for almost all programming except for those leading-edge functions that still benefit from differentiated, application-specific resources that a targeted processor might include.

As compilers improved, development tools underwent an integration effort not unlike that for SOCs (systems on chips). Integrated development environments grew into sets of many tools, including editors, compilers, debuggers, and profilers. The value of this integrated environment lies in the fact that it simplifies a developer's learning curve and shortens compilation and build time, especially as software continues to be an ever-larger portion of the development budget, not just for end-equipment designers but increasingly for semiconductor companies. These environments allow a developer to spread common tasks among targets so that the developer can focus on the differences between targets instead of differences in the development tools.

Semiconductor companies are also helping to hide complexity by allowing developers to choose their processor target later in the design cycle. Freescale's Flexis and Atmel's AVR lines blur the line between 8 and 32 bits by sharing common IP (intellectual property) between the processor groups. Microchip takes the same approach with some of its 16- and 32-bit PIC devices. Many other companies offer large device families that allow developers to move up and down through the family to size the target processor as late as possible in the design cycle. These abstractions or choices allow developers to focus on what function the design needs to perform and less on how to fit a chosen processor into the design.

Exploratory compilation is potentially emerging as a trend among compilers for complex signal-processing systems that can help offset the increasing complexity of software. Texas Instruments a few years ago implemented exploratory compilation for its VLIW (very-long-instruction-word) C64x processors that have eight execution engines that can operate in parallel. Ceva recently added a similar capability to its compiler tool set (**Figure 1**). The compilers perform multiple compilations of each function with different settings. These tools then present a developer with information about how the settings affect code size and performance so that the developer can fine-tune the results of the compilation. Academic variations on this concept can include profiler-based feedback that further refines the compilation settings.

Exploratory compilation and profiling feedback have greater potential as processor architectures become more complex with even more heterogeneous or homogeneous execution units. A compiler that can generate dozens, hundreds, or perhaps thousands of candidate configurations of the resources and code and then dynamically test and rank each of them would provide a significant level of abstraction to the developer. The system would also need to be able to provide confidence, maybe through mathematical proof, that the final candidate configurations are equivalent to the source code. Such a technology could also provide the essential capability for code reuse because the source code could focus on function and synchronization specifications while the compiler tries out many configurations on whatever resources the target processor supports.

To make all of these capabilities possible, hardware resources had to coincide with the software advancements. Further advancements in software tools will probably require as-yet-unknown specialized hardware resources. As a point of interest, this year saw two significant acquisitions of operating-system companies. Cavium Networks acquired Montevista, and Intel acquired WindRiver. These moves may signal an imminent inflection shift for operating systems and hypervisors to hide complexity from developers. EDN

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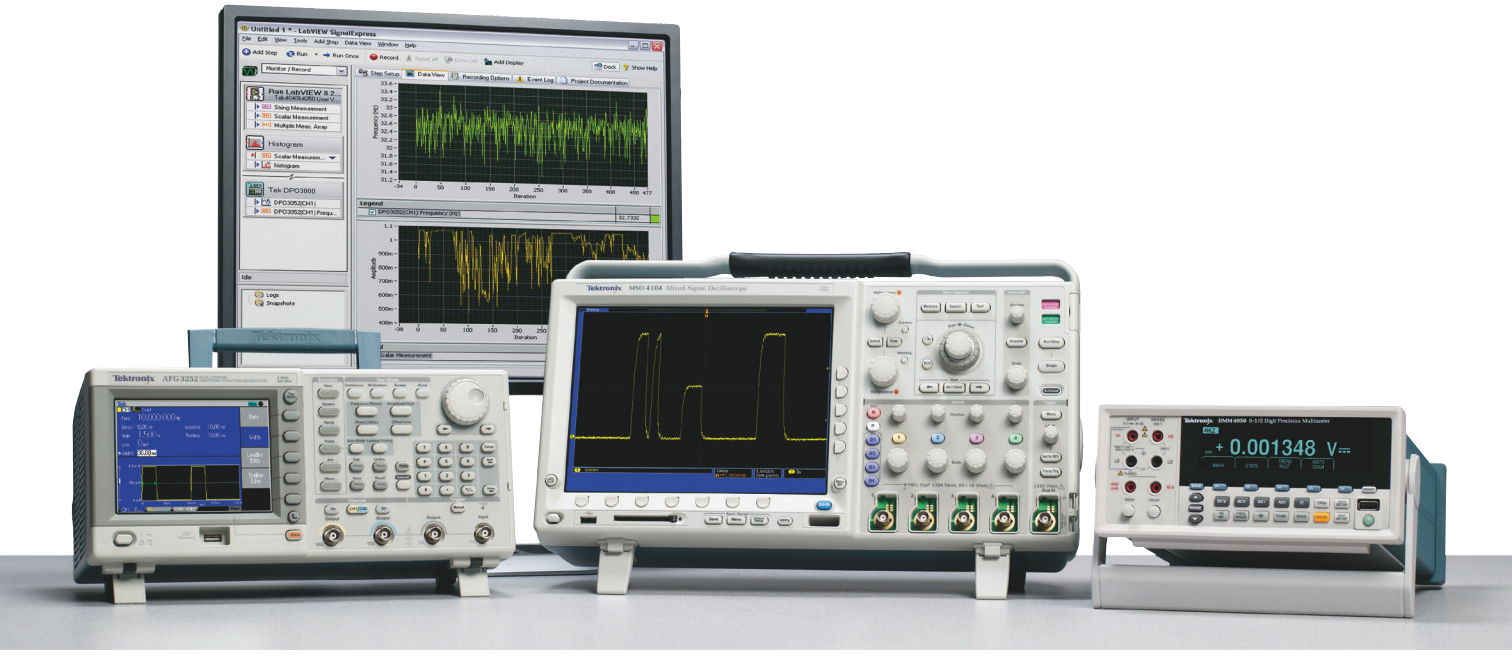

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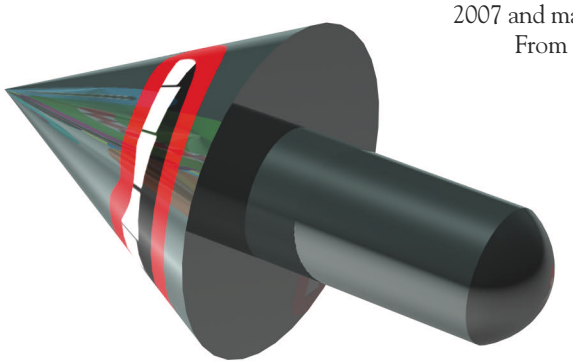
# INTEGRATION IN THE OTHER DIRECTION

BUILDING YOUR SYSTEM WITH SEPARATE DICE OR SEPARATE CHIPS MAY BE A SMART ALTERNATIVE TO USING SOCs.

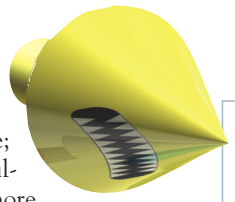
SOCs (systems on chips) have historically represented the Holy Grail for electronics because using these chips allows electronic-systems designers to pack a lot of digital circuitry into a small area. Nevertheless, fine-line CMOS does not suit use in analog, power, and RF functions, and tiny CMOS transistors are prone to noise and leakage problems. Further, the dedicated mask set you need to make the chip can cost more than $1 million. You then must commit to that design until high-volume sales amortize its costs. For these reasons, it sometimes makes more sense to use separate chips rather than pack everything onto one.

Dave Robertson, vice president of analog technology at Analog Devices, advocates employing "smart partitioning" rather than dictating a dogma for either integration or "disintegration"—that is, moving functions onto other chips. "You have to look at each case and pick the smart thing to do," he says. "The smart thing to do in 2010 was not the same smart thing to do in 2007 and may not be the same smart thing to do in 2013."



From a historical standpoint, no company would better exemplify the mistakes of choosing the wrong strategy for integration than Trilogy Systems, whose goal was to put an entire mainframe onto one wafer—the precursor of today's SOC. The company's $230 million in venture-capital funding was the "biggest start-up kitty ever," according to Myron Magnet, a former reporter for *Fortune* and now editor-at-large of *City Journal* (**Reference 1**). Trilogy eventually collapsed and became one of the biggest failures in Silicon Valley history after yield problems forced designers to implement redundant and corrective circuitry. This circuitry took up even more space, and the designers soon realized the near impossibility of testing such a gigantic system.

In other words, massive integration is not always the best option. "We look at what technology best fits," says Tim Kalthoff, chief technologist at Texas Instruments. "Some-



times, it makes more sense to use one die; other times, using multiple dice makes more sense."

Digital functions, such as memory cells, which require more process steps than CMOS logic can provide, also may benefit from a disintegration approach. For example, Samplify Systems makes ADCs with built-in data compression but implements analog functions, such as the low-noise amplifier for ultrasound, off-chip (**Reference 2**).

SiTime offers MEMS (microelectromechanical-system) oscillators that use clever leading-edge process technology that involves laying down silicon structures inside silicon oxide, or glass, capping the structure with polysilicon, and then dissolving the glass with hydrofluoric acid to create the cantilevered oscillator structure (**Reference 3**). The silicon process has circuitry on the same die to perform signal conditioning and other functions. It would make no sense, however, to implement all these process steps in a fine-line digital process so that you could integrate a MEMS oscillator onto an ASIC or an FPGA. This approach would invoke a cost penalty that would apply to the entire die.

The extra process steps for MEMS, analog, or memory also reduce the yields of the fine-line digital circuits. "We have MEMS parts with the sensor and signal conditioning on the same substrate," says Robertson. "In other parts, we disintegrate the sensor from the signal conditioner and put two substrates into one package."

Silicon transistors are not the best optotransistors because silicon has an indirect bandgap, which can reach maximum efficiencies of only 22% compared with 41% for direct-bandgap materials, such as GaAs (gallium arsenide, **Figure 1**). Researchers are trying to mix these processes by placing both germanium and gallium semiconductors onto a silicon die (**Reference 4**). Even if this research pans out in the real world, it will still be uneconomical to add the required process steps to large CMOS digital die.

In addition to their optoelectronic properties, GaAs semiconductors have higher electron mobility and larger bandgaps, which make them suited for use at RF frequencies. Cree, for example, cross-pollinates its expertise in III-V semiconductor LEDs; these semiconductors, in their intrinsic form, comprise atoms of one element belonging to Group III of the periodic table and of one element belonging to Group V. This cross-pollination takes advantage of the higher frequency capabilities of the process, and the company can apply research breakthroughs to its business lines.

### AT A GLANCE

- The decision to integrate or "disintegrate" depends on many dynamic factors.
- It may be better to implement analog, RF, MEMS (microelectromechanical systems), and optoelectronics functions in separate chips.
- Reducing inductance and power may require disintegrating your system.
- One large chip may be expensive or impossible for you to test.
- Modern packaging has changed the rules for integration.
- Trying to integrate everything onto one CMOS die can make you late to market and hurt performance and cost objectives.

## NOT READY FOR SOC

Faster processes always challenge silicon in the design of RF parts. The chips in a 2.4-GHz Wi-Fi hot spot almost certainly use just fine-line CMOS. When operating at 2.4-GHz and higher frequencies, however, transistors for digital processes have poor linearity, and the low-voltage range of fine-line CMOS means that your analog circuits will have little or no head room to compensate for that poor linearity (**Reference 5**). These limitations are among the reasons that many companies use a SiGe (silicon-germanium) process instead of a small CMOS process (**Reference 6**). Small CMOS transistors have thin oxide layers and therefore must run at low voltages. This approach works well in digital designs because the lower voltages also reduce power requirements. Many RF functions require you to broadcast RF, however, in turn requiring higher voltages than you can get from a fine-line CMOS process.

You can reduce the high leakage of fine-line CMOS by using a dielectrically

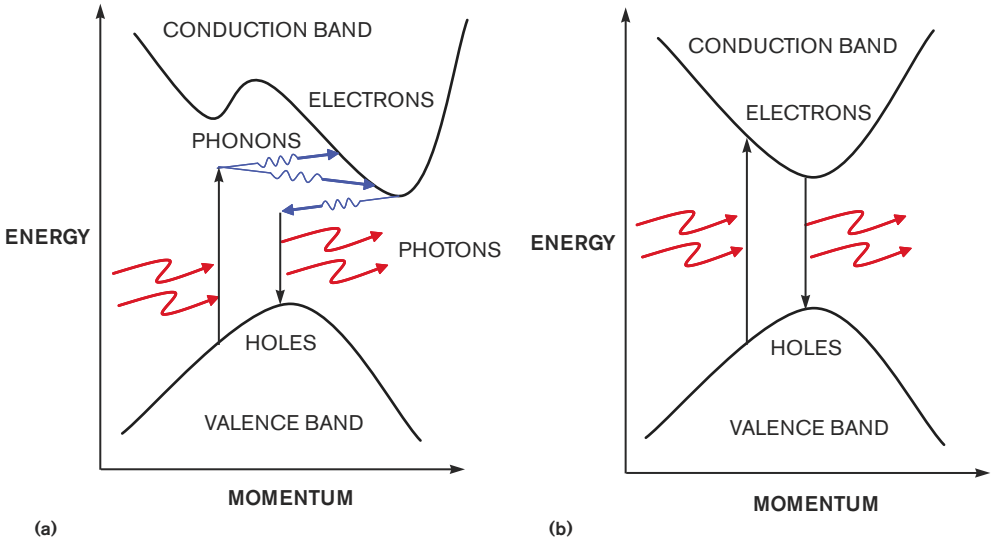



Figure 1 Silicon, an indirect-bandgap material, requires phonons, or lattice vibrations, to convert between photons and electron-hole pairs (a). GaAs and other III-V semiconductors are direct-bandgap materials and can achieve 41% efficiencies (b).

isolated silicon process, but that approach eliminates the technology's cost advantage. Because glass conducts 10 times less heat than crystal silicon, using glass to provide the dielectric isolation may cause a thermal problem. For this reason, Peregrine Semiconductor and others put CMOS onto a crystalline sapphire substrate that conducts heat three times better than glass. The lack of a silicon substrate also makes these companies' chips resistant to radiation.

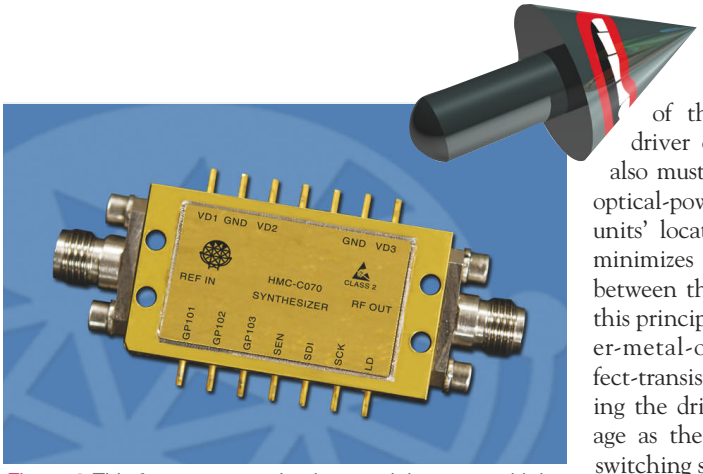



Figure 2 This frequency-synthesizer module uses multiple die with SiGe, GaAs PHEMT (pseudomorphic-high-electron-mobility transistor), and InGaP (indium-gallium-phosphide)-HBT (heterojunction-bipolar-transistor) processes in one module (courtesy Hittite Microwave).

Hittite Microwave bases its decisions about the level of integration on such factors as process capability; engineering talent; and market requirements, such as cost, volume, and design volatility. For example, the company makes high-performance microwave-synthesizer modules that use three processes in separate dice to provide the best performance (**Figure 2**). The company also makes PLL (phase-locked loop) parts that integrate two dice in one QFN package, using a GaAs process to get the best performance for the VCO (voltage-controlled oscillator) and a silicon die for the PLL function. Hittite believes that it is appropriate to use a CMOS IC if the application demands the low cost and compactness that consumer and end-user applications typically require. For example, a vehicle's radar detector typically uses one CMOS chip because the cost pressures make that approach the only viable one. Hittite's line of PLLs integrates CMOS operating at frequencies lower than 6 GHz and integrates a multidie part for higher frequencies. Using GaAs, on the other hand, enables you to implement VCOs that operate at frequencies as high as 26 GHz.

According to Steve Sockolov, analog-product-line director of precision amplifiers at Analog Devices, basic electrical reasons exist for implementing separate chips for different functions. "We have amplifiers at the edge of the board or on a connector, where customers demand 8-kV ESD [electrostatic-discharge] ratings," he says. "You can put those large ESD structures on a fine-line process, but it would not justify the cost." Many customers also demand power-supply overvoltage ratings of 40V, which fine-line processes cannot deliver, he notes.

Hubert Engelbrechten, chief executive officer at analog-signal-processing start-up GTronix, notes that using separate chips for signal conditioning saves power and reduces latency (**Reference 7**). The read-head amplifiers in disk drives, for example, must be on the moving read head to reduce noise and lower the impedance of the signal to the rest of the system. The laser-driver chips in DVD players also must reside on the moving optical-power units because the units' location close to the load minimizes the trace inductance between them. Fairchild employs this principle in its DrMOS (driver-metal-oxide-silicon-field-effect-transistor) parts. Incorporating the driver in the same package as the power FET improves switching speed.

ADSL (asymmetrical-digital-subscriber-line) amplifiers from Analog Devices work with transformers that must send 40V signals across twisted-pair phone lines (**Figure 3**). Using a large step-up transformer to perform this task would allow the use of low-voltage amplifiers but would also decrease the incoming signal and system performance. The Analog Devices ADSL amplifiers instead operate from 12 or 24V so that the transformers can keep a nearly 1-to-1 ratio of primary to secondary windings. The ADSL drivers also provide protection from lightning strikes on the phone lines, which can turn into 1-msec, 6A surge currents at 30 to 50V. A CMOS-process-derived part could not withstand surges of this magnitude, says Jim Doscher, product-line director of high-speed networking amplifiers at the company.

You must also consider the requirements of your system when you implement multiple chips. "You don't want to run a regulated voltage across the hinge of a cell phone," says Dan Swan, standard-power-product-line director at Analog Devices. The benefit of placing voltage regulators close to the load is equally valid in large data servers with hundreds of power-supply rails, he adds.

"For both performance and power consumption, we've proved that a disintegrated analog front end with two processes can gain from both worlds," says Danny Kreindler, director of marketing for medical and imaging products at Samplify Systems. Samplify integrates 16 ADC channels—but not the analog low-noise and programmable-gain amps—into one chip. Vendors of single-chip products tried to convince customers that using one chip would be less demanding because this approach uses fewer compo-

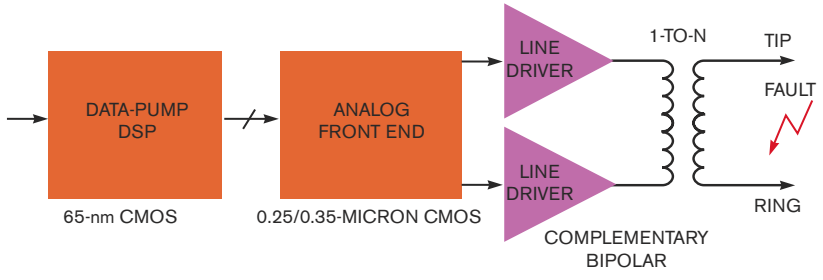



Figure 3 The high-voltage output and fault tolerance of ADSL modems require you to use different chips in the signal chain (courtesy Analog Devices).

nents, simplifies the design, and relieves customers of worries about impedances and coupling. "The single-chip vendors would say, 'Here is a chip and data sheet. Go!'" he notes. "It worked to get people to design in the chips, but I now see customers designing out single-chip solutions after seeing that [the other approach] looks good only on paper." Kreindler adds that a multichip system can achieve lower power consumption, often with a smaller board, than a single-chip approach. Samplify is countering the ease-of-design issue by offering demonstration boards and software that allow customers to evaluate their systems.

Power savings is another reason for choosing disintegration. "You have to look at the system as a whole and think of the best way to save power for the entire system," says Analog Devices' Swan, who provides an example in which a low-power chip can sense motion using an onboard accelerometer. The power-management chip in this scenario would then light the backlight and enable the circuitry that detects that a user is activating a key. In that way, you would waste no power running the big digital chips until you need them. For the same reason, Wolfson Microelectronics partitions handset electronics to incorporate an audio subsystem and the power management onto one analog IC.

Even in the purely digital domain, cell-phone designers divide systems into two large chips: the baseband processor and the application processor. The RF baseband chip is a real-time operating system that demands low latencies and lack of interruptions. The application processor can act more like the operating system on your desktop, in which millisecond latencies are not problematic. "The baseband chips are so busy doing error correction and demodulation of these complex protocols that a separate chip must do the user functions," says Paul Greenland, a power-management consultant. Greenland notes that you cannot use the voltage and current characteristics of tiny fine-line CMOS transistors for many analog functions. "You can make a digital PWM [pulse-width-modulated] loop in one-fourth or one-sixth the die area of an analog PWM loop," he says, noting that digital power is ideal in some medical and industrial markets. In these applications, digital power can provide the margining and fine control, but this approach involves a development-cost issue. For example, an 8-in. fine-line CMOS mask set costs $1.2 million to $1.4 million, meaning that your digital-power chip must target high-volume markets to amortize that cost over a lot of chips.

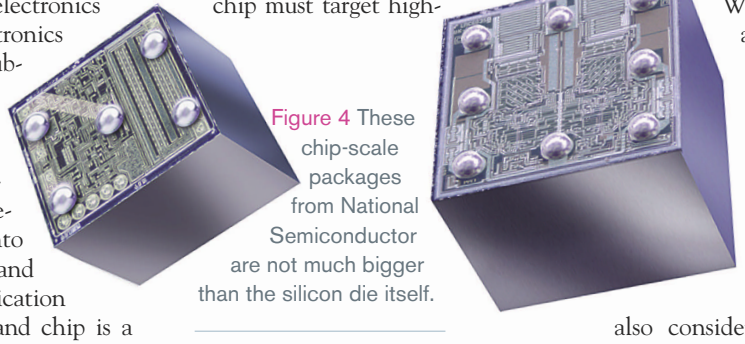



Figure 4 These chip-scale packages from National Semiconductor are not much bigger than the silicon die itself.

Exar takes this approach with its digital-power chips for set-top boxes and servers. The company's IP (intellectual property) and patents often involve methods of making small dice. The company integrates the charge pump's high-side drivers—but not the power FETs—into the chip. With such a small die, the chip can compete with analog products and offer all the programmability and communications capability of a digital chip.

## TESTING, TESTING ...

Market definition, system partitioning, and IC design are just some of the jobs you must complete before you get a product into your customers' hands. You must also test that product all through the manufacturing process, and this testing and the design of the test systems involved can be major parts of introducing a chip, says Jim Williams, staff scientist at Linear Technology. You cannot use inexpensive digital testers to test high-end, sophisticated analog chips, such as those from Linear Technology. The probe card that holds the chip under test is often customized for that chip. "It is not uncommon that controlling items in the release of a new part are the design and building of the test system," says Williams.

A large semiconductor company recently learned the nuances of analog testing when it moved all product testing to standard digital machines. The designers of the probe cards and test routines in the high-performance analog division had retired. With poor documentation and exotic circuits beyond the ken of the company's digital-test engineers, the task of running all chips on standardized testers soon turned into a disaster that took more resources than the company had anticipated.

Beyond testing, you must also consider packaging for your design. When ICs came in 40-pin ceramic packages, adding a chip to your design brought about a huge cost and PCB (printed-circuit-board)-area penalty. These days, however, the packages are no bigger than the dice inside them. Most analog-product vendors offer parts in chip-scale packages, essentially including the die and the solder bumps on the metallization to mount the part on your board (**Figure 4**). Putting the functions into separate parts allows for flexibility in process choice and board location that may be essential to meeting your design goals.

Many companies put many dice into one package to reap the benefits of pro-

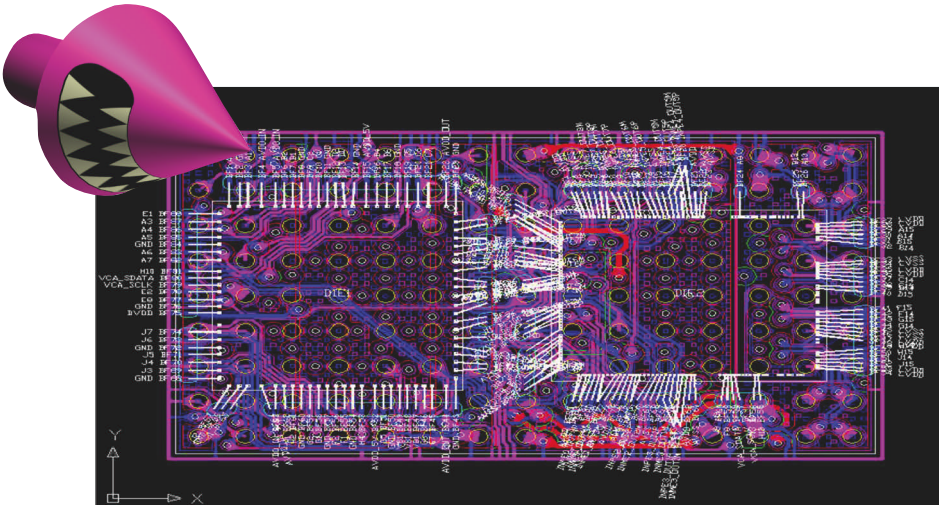


Figure 5 This analog front-end IC for medical-ultrasound machines combines a SiGe low-noise amplifier die and a CMOS data-converter die into one package (courtesy Texas Instruments).

cess and die-substrate variations and the convenience and size benefits of a single package. Texas Instruments offers an ultrasound analog front end comprising two dice on one package (**Figure 5**). The company uses a SiGe process for low noise and CMOS for digital-processing and ADC functions. Similarly, Linear Technology sells quad op amps that comprise two dual op amps in the same package. The company recently created an RS-485 isolated-driver module that incorporates multiple chips, along with transformers for isolation and power (**Reference 8**). Linear Technology has also inserted many of its RF parts into micromodules, in some cases using competitors' SAW (surface-acoustic-wave) filters. Analog Devices, meanwhile, offers a series of isolators that use two ICs and a separate spiral transformer. "The packaging technology has changed the rules a lot over the last 10 years," says Robertson. "The next 10 years will see through-silicon vias and other packaging technologies change the integration rules again."

From all these arguments and counterarguments, you can see that the goal of integration or disintegration is a moving target. If your system is in a settled market with consumer cost pressures and modest performance demands, then an integrated fine-line CMOS process is your best bet. Even settled markets are dynamic, however. A Wi-Fi chip may perform the RF and digital processing necessary in today's market. If you need a router that performs deep packet inspection to discard spam or thwart hackers, however, you may wish that you had broken that design into smaller parts (**Reference 9**).

Die and mask costs, process capability, and engineering efforts are all changing monthly. What is now available at your company may differ from what is available to your competitor. If your company has analog-design experts, it may be better off sticking to disintegrated designs. Your competitor, on the other hand, may decide to put everything onto one chip. The market will decide the ultimate winner, but make sure to understand all the implications of system partitioning and that every situation and every market is different. "That's what makes the job so interesting," says Analog Devices' Robertson. "Even if you are attacking the same end-application problem as you were three years ago, the toolbox changes every couple of years, so there are different ways to attack the problem, and the trade-offs become different." System partitioning and work flow are real-world problems, and the real world is always analog, even if your system is purely digital. That fact is what makes integration and disintegration so challenging—yet so rewarding when your hunches play out. EDN

## FOR MORE INFORMATION

**Analog Devices**
www.analog.com

**Cree**
www.cree.com

**Exar**
www.exar.com

**Fairchild Semiconductor**
www.fairchildsemi.com

**GTronix**
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**Hittite Microwave**
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**Samplify Systems**
www.samplify.com

**SiTime**
www.sitime.com

**Texas Instruments**
www.ti.com

**Trilogy Systems**
http://en.wikipedia.org/wiki/Trilogy_Systems

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www.wolfsonmicro.com

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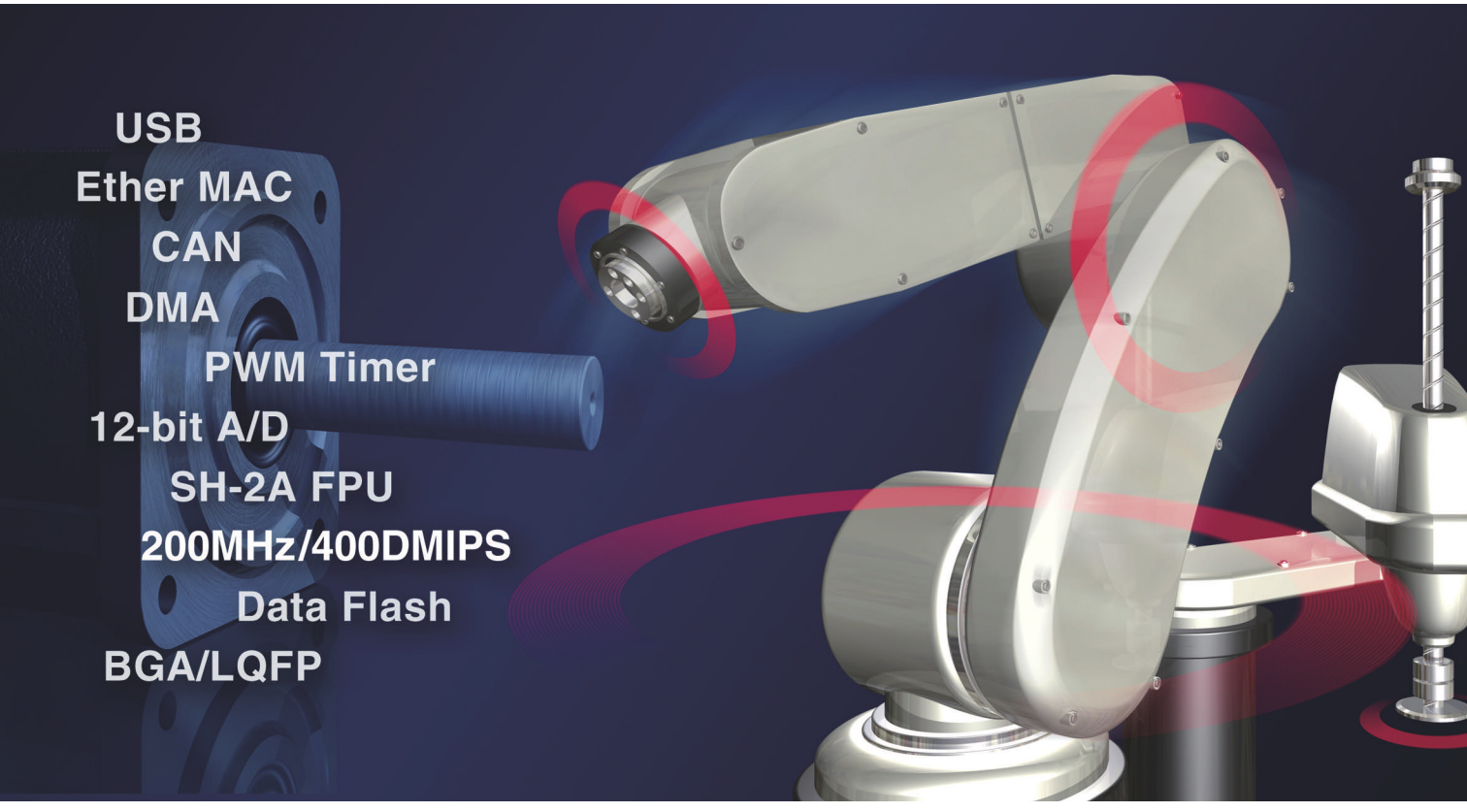


The SH7216 boasts a maximum operating frequency of 200MHz/400DMIPS* and a broad range of communication channels including Ethernet, USB and CAN. Additionally, optimized peripherals are included for realizing advanced motor control applications in AC servos, factory automation equipment and general purpose inverters.

### Key Features

- 200MHz/400DMIPS* high-speed SH-2A CPU core and single-cycle embedded flash memory eliminates the need to execute from RAM.
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- Various communication channels including Ethernet, CAN, and USB2.0 (full speed) device.
- 72 different family members, including various combinations of frequency, memory capacity, packages including BGA and LQFP, and options both with and without FPU or Ethernet.
- Peripherals optimized for industrial equipment, including two PWM timers and 12-bit A/D converters with 1 µs conversion time.
- A 32KB data flash with Background Operation (BGO) function, meaning there is no need for external EEPROMs.

*Note: 400DMIPS is measured based on Dhrystone software executed from on-chip flash.

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# designideas

READERS SOLVE DESIGN PROBLEMS

## Excel spreadsheet measures analog voltages

Yury Magda, Cherkassy, Ukraine

You can use the parallel port, which many computers still have, with some VBA (Visual Basic for Applications) code and Microsoft (www.microsoft.com) Excel 2007 to measure, record, and analyze analog signals. The hardware comprises a 12-bit Microchip (www.microchip.com) SAR (successive-approximation-register) ADC (**Figure 1**). The binary code that represents this signal passes to the parallel port through an SPI (serial-peripheral-interface)-compatible port, which includes three signal lines.

The analog input signal on Pin 2 of the MCP3201 ranges from 0 to 5V. The ADC's reference voltage is 5V, which provides an LSB (least-significant bit) of $5/2^{12}$, or 1.2207 mV. You can substitute the MCP3201 ADC with the Linear Technology (www.linear.com) LTC1286 chip, which is pin-compatible with MCP3201, but this replacement requires some changes in the source code. The circuit includes a 1- to 10-µF bypass capacitor that you should place as close as possible to the MCP3201's power pin. You can improve performance by placing a lowpass active filter between the signal source and the converter's input (Pin 2).

The design uses the PC's default parallel interface, $LPT_1$, which has three hardware registers: data, status, and control. Most PCs have only one parallel port with the base address 0x378 assigned to the data register. The status register has the address 0x379, and the unused control register has the 0x37A address. These settings are the defaults for most motherboards. This design uses addresses 0x378 and 0x379. The parallel port sometimes uses hardware addresses in the range of 0x278 to 0x27A. The hardware addresses may also vary when you apply a PCI (Peripheral Component Interconnect) expansion board with a built-in parallel interface. You should check the hardware addresses of the selected parallel interface and set appropriate values in the source code.

The program uses the inpout32.dll library, which is free and accessible for downloading at www.logix4u.net. The inpout32.dll includes two useful functions, `Inp32` and `Out32`. The `Inp32` function reads a data byte from the hardware register (`port`), and `Out32` writes the byte into the hardware port. Before using the inpout32.dll, you should copy the inpout32.dll into the \system32 directory so that the VBA application can find it. You can download **Listing 1**, the VBA code, from the online version of this Design Idea at www.edn.com/100121dia.

To write a VBA control program, you should create a new Excel workbook and open the Visual Basic editor where you enter the source code. After doing so, you must insert a new user form (**Figure 2**). You need to drop a button component from the toolbox onto the user form. When the application is running, clicking the button causes the value of the analog voltage to appear in the current cell of Column A of Spreadsheet 1.

You should declare functions `Out32` and `Inp32` from the inpout32.dll library with the `Declare` directive so that the application can use them. The `Out32 (port, portVal)` holds the hardware address of the port to write data to. The value of the byte goes in the `portVal` parameter. The `Inp32` function

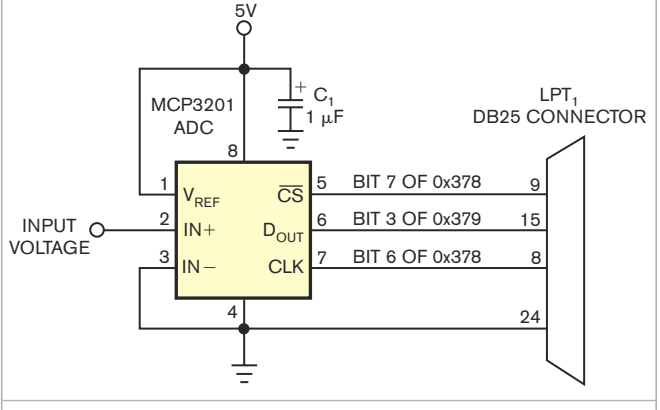


Figure 1 An MCP3201 ADC digitizes the input voltage.

### DIs Inside



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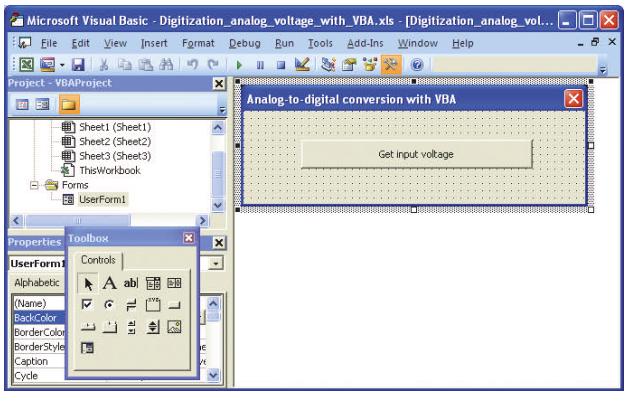


Figure 2 You can create a user form with a button to execute the conversion.

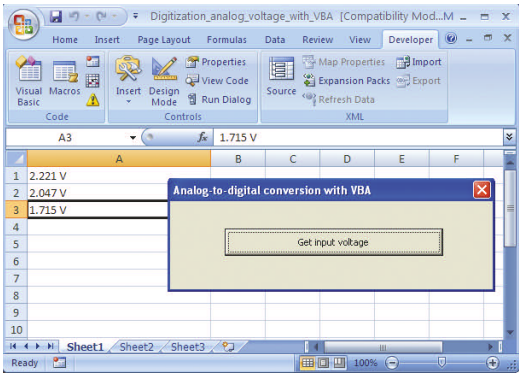


Figure 3 The VBA application collects data in an Excel spreadsheet.

takes the `port` parameter where the address of the port is held. When successful, this function returns the byte read from this port.

The program realizes the timing diagram of the conversion and outputs data when the `CommandButton1_Click` event handler is called. The statements

```
Call Out32(dataPort,
&H80)
Call Out32(dataPort,
&HC0)
Call Out32(dataPort,
&H40)
```

start the conversion. The `for()` loop passes data bits beginning from the MSB (most-significant bit) to the parallel port. The 12 bits of the result are saved in the `binData` variable, and the total variable holds the final result. **Figure 3** shows the main window of the running application. After you click the "get input voltage" button, the measurement result appears in the next cell in Column A of Spreadsheet 1. EDN

# Schottky diodes improve comparator's transient response

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

In a previous Design Idea, a circuit switches precision dc reference voltages to the noninverting input of a high-speed IC comparator (**Reference 1**). The circuit uses a 2-to-1 multiplexer that functions in a BBM (break-before-make) fashion. Multiplexers have a parasitic capacitance, whose injection of charge, $Q_{D1INJ}$, into the D1 drain electrode of the multiplexer might cause error voltages at the comparator's reference input (**Figure 1**). The following **equation** defines the approximate peak error voltage:

$$\Delta V_{D1+} \simeq \frac{Q_{D1INJ+}}{C_{D1OFF} + C_{IN}},$$

where $C_{D1OFF}$ is the capacitance of the D1 terminal of $IC_2$, and

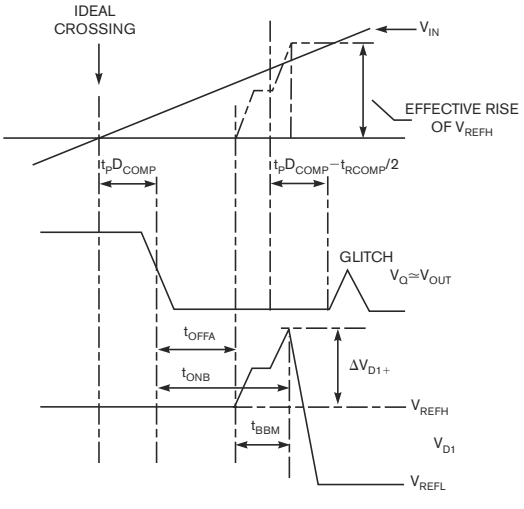


Figure 1 Charge injection can produce a glitch in a voltage comparator's output, and these glitches can cause logic hazards.

$C_{IN}$, approximately 1 pF, is the input capacitance of the comparator. $IC_2$ has a BBM interval of approximately 3 nsec, and any Analog Devices (www.analog.com) ADCMP608 and ADCMP609 comparators' signal-propagation delays are 10 times that value. Hence, they cannot change their state in 3 nsec. Analog Devices has 10-times-faster parts, the ADCMP601 and ADCMP602, in the same family. Unfortunately, these devices can sense these spikes (**Reference 2**). The voltage excursion over the high-level reference voltage, $V_{REFH}$, can result in an abrupt short-term elevation of the output voltage.

When the high reference voltage exceeds the voltage at the comparator's inverting input, its output goes high again, or generates a glitch. As the comparator crosses an ideal level, the comparator's output goes low with a delay. The positive error voltage starts to evolve with an additional delay of the

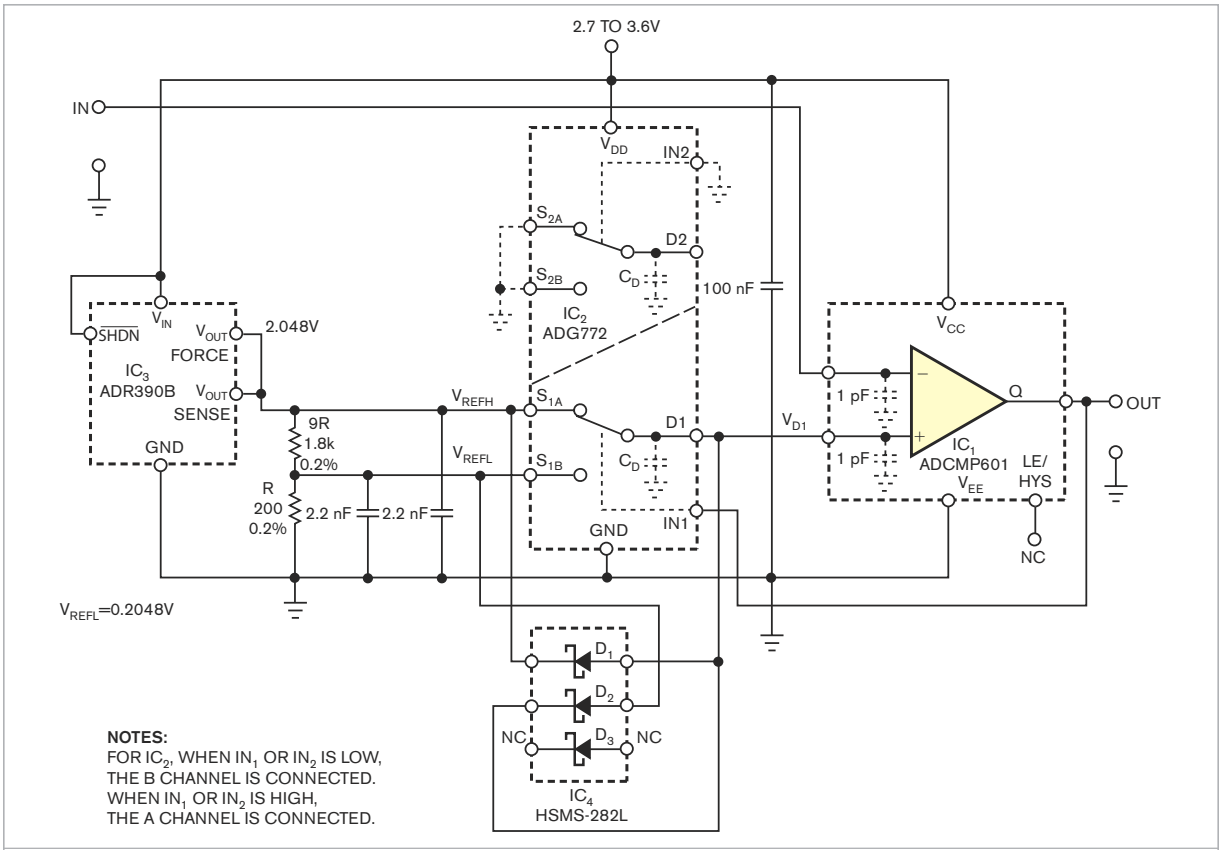


Figure 2 Schottky barrier diode $D_1$ damps positive voltage spikes that occur at the noninverting input of comparator $IC_1$ shortly after the high-to-low transition of the output voltage. Diode $D_2$ clamps the negative excursion of the reference voltage during a low-to-high transition of the output voltage.

turn-off time of Channel A of $IC_2$. The ADCMP601's data sheet shows a charge injection into the source electrode. In this case, however, charge injection to the drain electrode plays a role. As a rough estimate, you can use the data on charge injection in **Reference 2**. As the charge injection changes its sign, depending on the value of the common-mode voltage, the charge is about 0.8 pC at $V_{D1}$, which equals the high-level reference voltage, and it is approximately −0.3 pC when the reference voltage is low. This voltage ceases with the delay of the turn-on time of the channels in analog switch $IC_2$, an ADG772 (**Reference 3**). The inadvertent return of the comparator's output to high, although lasting no more than 5 nsec, might cause some logic circuits to respond unexpectedly. A similar situation might occur when the input ramp with a negative slope crosses the lower reference voltage.

To prevent these hazardous states, you can add two Schottky barrier diodes (**Figure 2**). Diode $D_1$ starts to conduct whenever a positive voltage excursion of approximately 200 mV above the higher reference voltage occurs at the D1 terminal, whereas $D_2$ conducts at excursions of 200 mV below the lower reference voltage. Further, the nonlinear junction capacitance of these diodes rises with forward voltage from 0.7 pF at a forward voltage of 0V to approximately 1.05 pF at a forward voltage of 100 mV. At input voltages close to the higher reference voltage, diode $D_2$ is reverse-biased by almost 2V, and its capacitance drops to approximately $2/3C_D(0)$, where $C_D$ is the capacitance of the nonbiased diode. Diodes $D_1$ and $D_2$ have a combined capacitance of 1.5 pF. This amount can increase the input capacitance. Because the charge injection doesn't exceed 0.8 pC, the voltage excursions at the D1 terminal are less than 160 mV. Diodes $D_1$ and $D_2$ reside within diode trio $IC_4$, an Avago Technologies (www.avagotech.com) HSMS-282L (**Reference 4**), but you can also use a diode-pair IC. EDN

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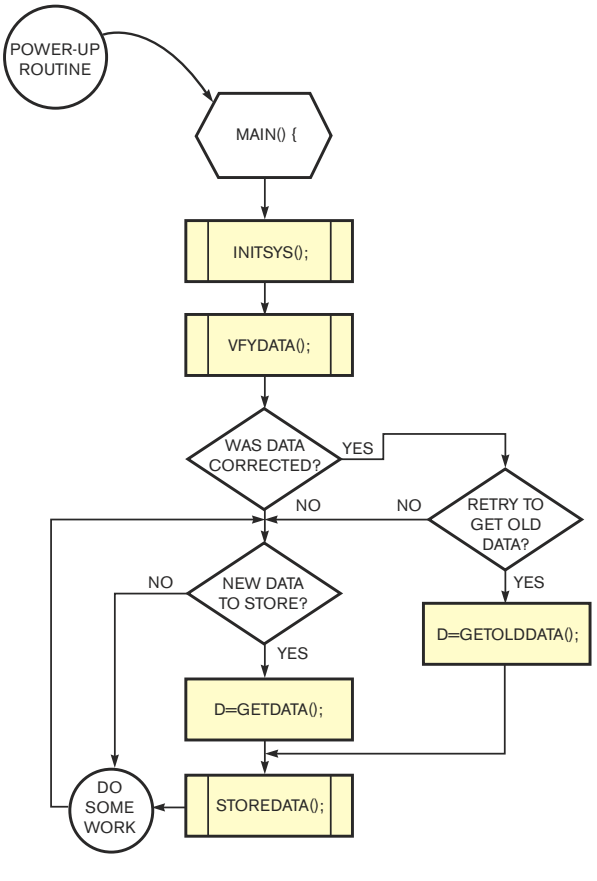
# Algorithm keeps data safe

Luis G Uribe C, Caracas, Venezuela

Many embedded systems must regularly update multibyte data to EEPROM, flash memory, or a database server. This Design Idea presents a robust algorithm for this process that prevents data losses and inconsistencies due to program interruptions or power failures. You can avoid data losses by maintaining two separate memory areas, duplicating critical variables in each. Memory can be battery-backed RAM, magnetic disks, flash memory, or local or remote storage subsystems. You can use a simple FSM (finite-state machine) that uses three or four states with appropriate Gray coding to track the status of each main variable and its mirrored value in the storage devices. The states run in a sequence that the software driver can use to write data to both the main and the backup variables. The driver sets and resets two variables, B0 and B1, as status bits. B0 is the main variable status bit, and B1 is a mirror status bit. Both bits are recorded in the same storage medium as the data.

This algorithm prevents race conditions and ambiguous situations. You can enter the power-up verification routine at any time, interrupting the main flow of the program without losing any data. **Figure 1** shows the flow of the algorithm, which begins with a power-up routine. **Table 1** identifies and defines each of the possible states for the variables. EDN




**NOTE:** TRYING TO RETRIEVE OLD DATA THAT WAS NOT STORED IS HIGHLY DEPENDENT ON THE APPLICATION.

Figure 1 This algorithm starts with a power-up routine and then verifies that the data is properly stored. (For other algorithms, go to www.edn.com/100121dib.)

**TABLE 1 POSSIBLE STATES OF VARIABLES**

| Bit state | | Description |
|---|---|---|
| B0 | B1 | |
| 0 | 0 | Both variables are in steady state. |
| | | If the power-up routine finds this state, it may assume that everything is fine; both values are properly stored in the main site and in the backup. Your program may read and use the data as needed. |
| | | When it's time to modify a value, the driver sets a one at B0 to indicate a zero/one. |
| 0 | 1 | Data begins to write to the main variable. |
| | | If the power-up routine finds this state upon verification, you can assume that the main variable is corrupt and decide how to update it from the mirroring site. |
| | | When the driver finishes updating the main variable, it sets a one at B1 and keeps B0 untouched at one to indicate two ones. |
| 1 | 1 | Data has written properly to the main variable, and the driver soon begins the next state to duplicate main data into its backup storage. |
| | | This state is transient to avoid changing bit values between zero/one and one/zero at once. Using this sequence, the two data repositories may be in different local or remote physical subsystems. |
| | | If the power-up routine finds this state, it may assume that the mirror variable is corrupt, and it will proceed (next state) to update the mirror site from the main location. |
| | | At any convenient time from now on, the finite-state machine may leave this state and enter the next one, one/zero, which means: |
| 1 | 0 | Data has properly written to the main variable state, and the driver now begins to duplicate the main data into backup storage (similar meaning to previous state, one/one). |
| | | If the power-up routine finds this state, the verification routine may assume that the mirror variable is corrupt and update the mirror site from the main variable. |
| | | When the driver finishes updating the mirroring variable, it clears B1, and the finite-state machine reverts to the first state, two zeros, in the sequence. |

# Industry's smallest and smartest touch-screen controllers

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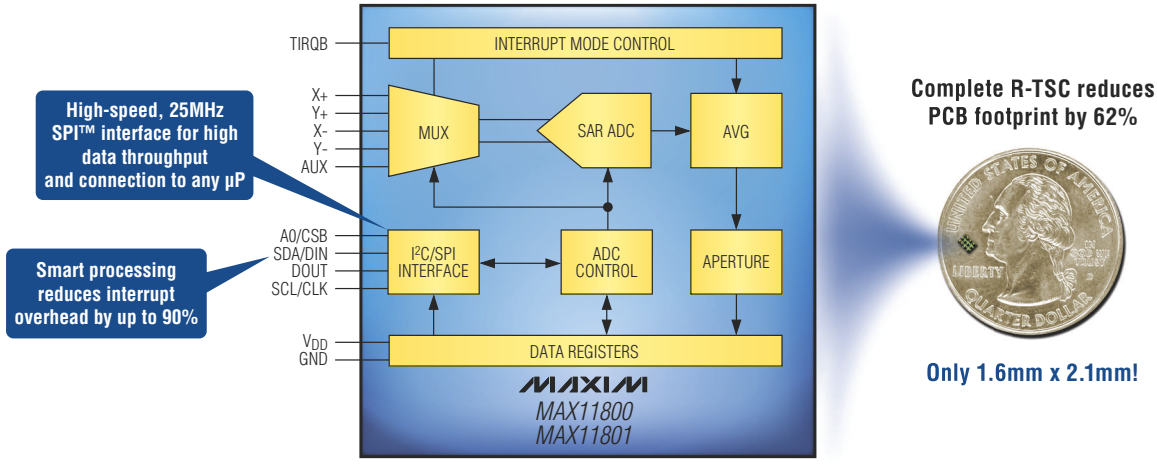
The MAX11800/MAX11801 are resistive touch-screen controllers (R-TSCs) available in TQFN and ultra-small WLP packages. These devices have advanced operation modes and other digital functionality that reduce bus loading of the system/applications processor, plus numerous advantages including the reduction of necessary board space and the ability to connect to any host µP. Ideal applications include mobile phones, MP3 players, personal navigation devices (PNDs), ultra-mobile PCs (UMPCs), office printers, gaming consoles, and digital photo frames.

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- **FIFO increases effective throughput**
- **Programmable scan rate allows tradeoff between power and accuracy**
- **Data-tagging identifies type of measurement (X, Y, pressure) and type of touch event**
- **Programmable averaging reduces noise**

| Part | Interface | Temp Range (°C) | Package (mm x mm) | Price† ($) |
|---|---|---|---|---|
| MAX11800ETC+ | SPI | -40 to +85 | 12-TQFN (4 x 4) | 1.55 |
| MAX11800EWC+ | | | 12-WLP (1.6 x 2.1) | 1.51 |
| MAX11801ETC+ | I²C | | 12-TQFN (4 x 4) | 1.50 |
| MAX11801EWC+ | | | 12-WLP (1.6 x 2.1) | 1.46 |

SPI is a trademark of Motorola, Inc.
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# P-channel power-MOSFET driver uses unity-gain op amp

Suded Emmanuel, Emmanuel's Controls, Auckland, NZ

P-channel MOSFETs can simplify designs when you use them as high-side switches on circuits with voltages exceeding 100V dc. When driving a MOSFET, you must rapidly charge and discharge the input capacitance between its gate and its source to reduce heat losses. The circuit in **Figure 1** can accomplish that task. $Q_7$, an International Rectifier (www.irf.com) IRF5305 power P-channel MOSFET, switches 50V to a load. A series of pulses from a pulse generator or PWM (pulse-with-modulation) source drives the load at frequencies as high as 60 kHz with a variable duty cycle. The circuit comprises $Q_4$, $R_5$, $D_2$, $R_4$, $D_3$, and $R_3$; provides a means of level-shifting; and ensures that the voltage drop between the gate-to-source voltage of $Q_7$ never exceeds 10V. When $Q_4$ is on, 10V develops across $D_3$. This voltage drop turns on $Q_7$ through op amp $IC_{1A}$, one-half of an MC33072 from On Semiconductor (www.onsemi.com). $IC_{1A}$ has a 13V/µsec slew rate and can drive capacitances as high as 10 nF.

The combination of $D_4$, $R_1$, $Q_1$, $Q_2$, $R_2$, and $C_1$ provides "ground" for the op amp, which is at 38V—that is, 12V below the 50V rail voltage. The positive voltage is 50V, and ground is 38V. The anode of $D_3$ connects to the noninverting input of $IC_{1A}$, whose output drives $Q_7$'s gate at 40V, which is 10V below the rail voltage of 50V. The circuit comprising $R_6$, $Q_5$, $D_1$, $R_7$, $R_8$, $Q_6$, $R_9$, $R_{10}$, and $Q_3$ rapidly switches $D_3$'s anode to 50V, which turns off $Q_7$. Transistor $Q_5$ functions as an inverter that turns on $Q_6$, which subsequently drives $Q_3$ to rapidly switch $D_3$'s anode to 50V and thus drives $Q_7$'s gate. Schottky diodes $D_1$ and $D_2$ alternately enhance the switching speed of $Q_5$ and $Q_4$.

Unity-gain op amp $IC_{1A}$, with its high slew rate, fast settling, capacitive-driving capability, and feedback of the gate voltage, enhances $Q_7$'s switching speed. Using this circuit, you can achieve a rise time and fall time of approximately 500 nsec at $Q_7$'s output. EDN

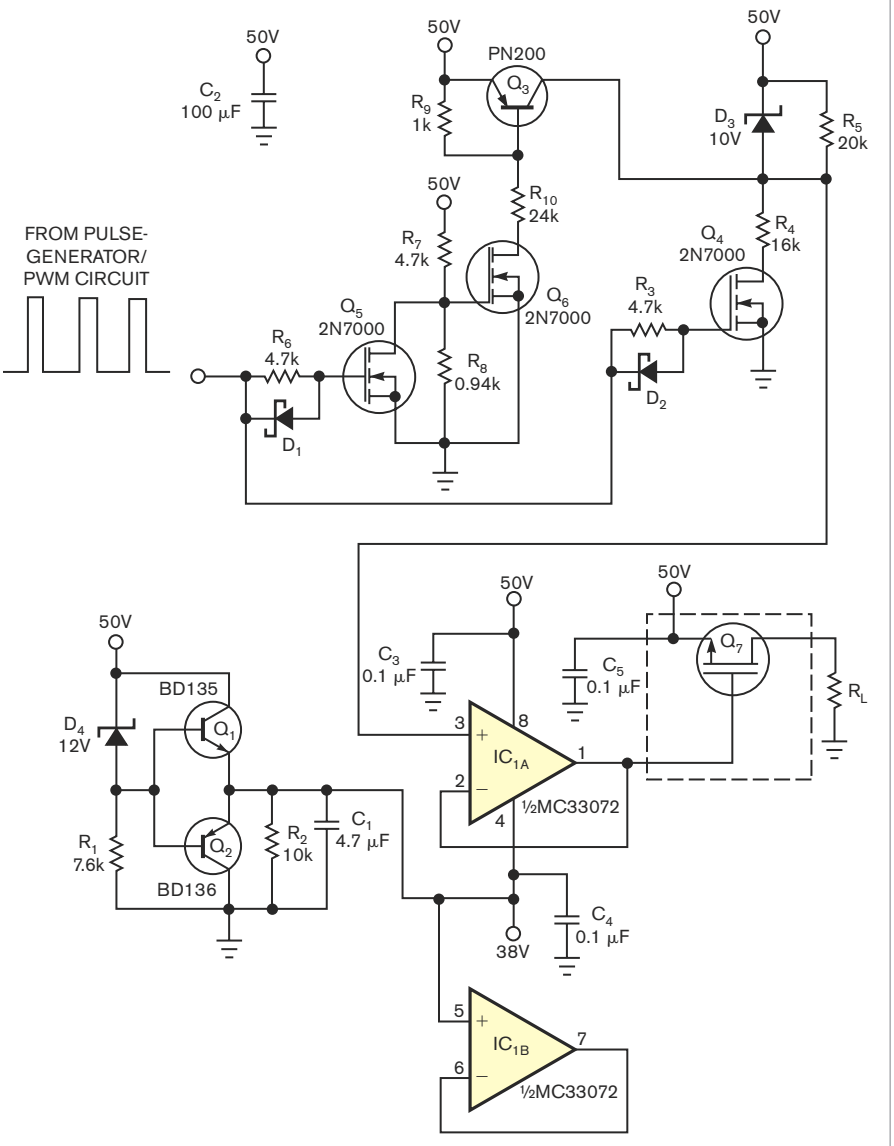
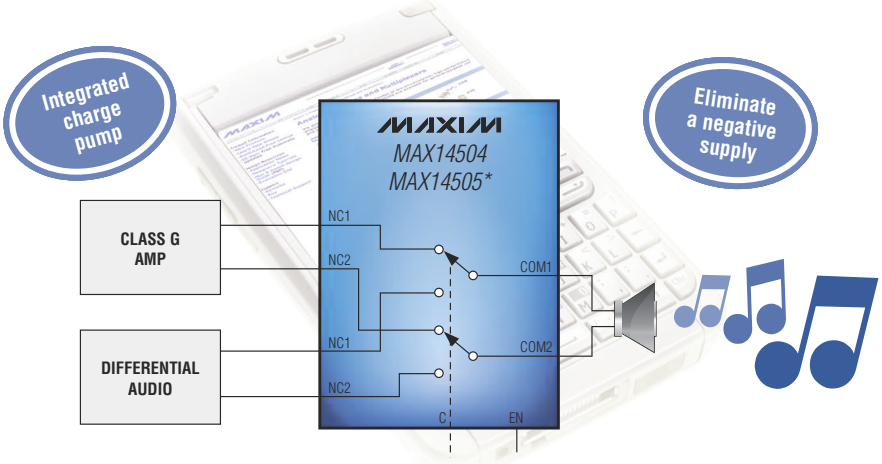


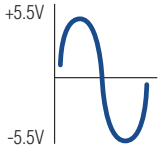

Figure 1 An op amp operating at 38 to 50V provides power to a load through power-MOSFET $Q_7$.

# Only single-supply switches with $\pm V_{CC}$ signal handling

The MAX14504/MAX14505* integrate a charge pump to support the high output-signal range required by Class G and DirectDrive® amplifiers. They thus enable the use of more-compact amplifier topologies while eliminating the need for a negative supply. Offered in a tiny wafer-level package (WLP), these devices allow you to add premium features when space is at a premium.




**Compatible with Class G or AC-coupled loads**




**Low 0.2µA shutdown supply current**


**Space-saving package**


## Support high audio quality

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- Low 0.05% THD+N
- Integrated shunt resistors available for click-and-pop suppression

## Ideal for portable applications

- 2.5V to 5.5V single-supply operation
- Low 0.2µA shutdown supply current
- Tiny 12-bump WLP

| Part | Configuration | Shunt Resistors | Signal Range | Package (mm x mm) |
|---|---|---|---|---|
| MAX14504 | Dual SPDT | — | $-V_{CC}$ to $+V_{CC}$ | 12-WLP (1.56 x 2.14) |
| MAX14505* | | NO and NC input | | |
| MAX14505A | | NO and NC input | 0 to $+V_{CC}$ | |
| MAX14506* | | — | | |

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.
*Future product—contact factory for availability.

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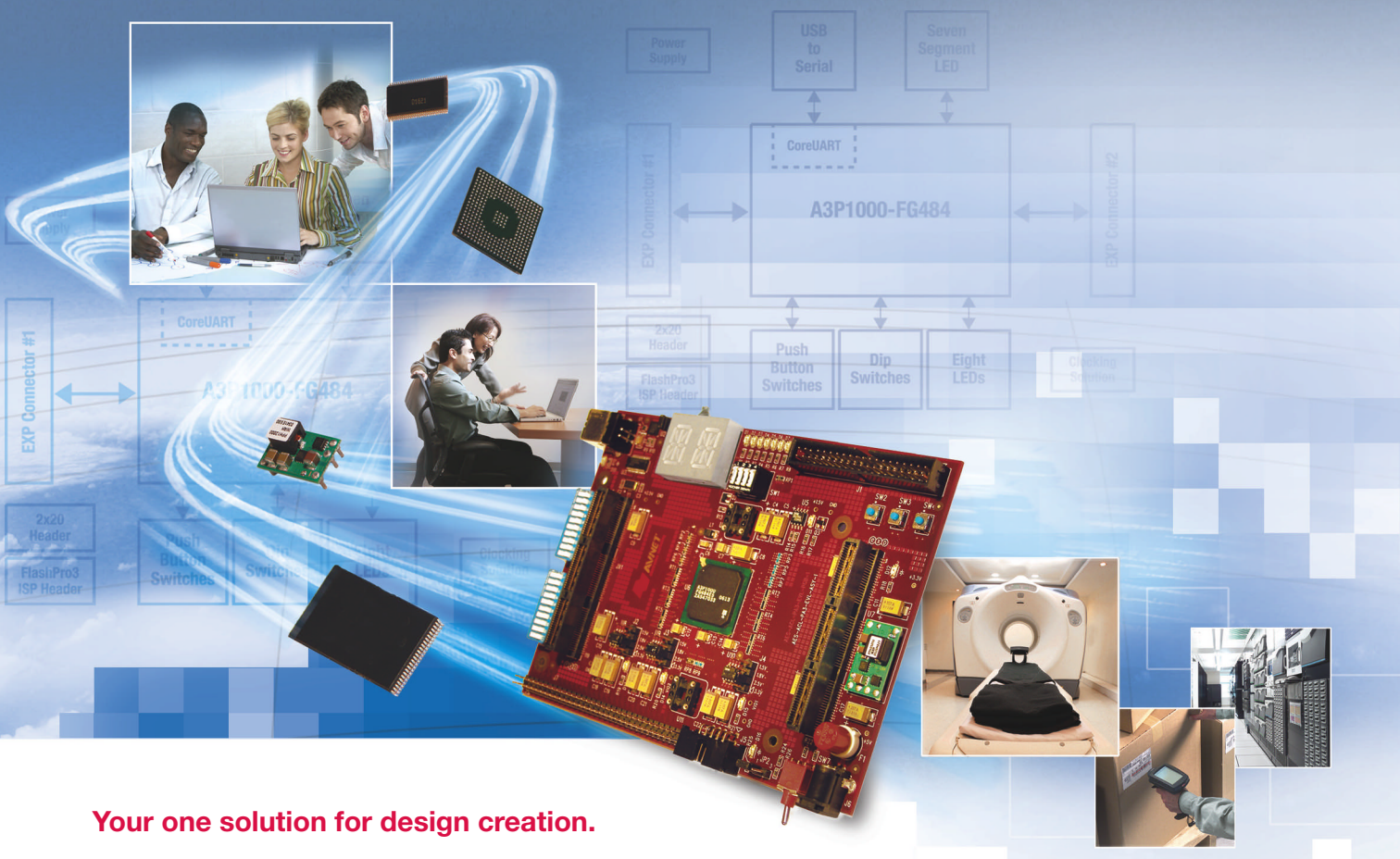


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# productroundup

## OPTOELECTRONICS AND DISPLAYS


### RGB laser driver targets embedded pico projectors

The three-channel MAX3600 RGB laser driver enables the integration of high-resolution pico projectors into small-form-factor applications. Built using the vendor's BiMOS process, the device achieves a switching time of less than 2 nsec, supporting high-resolution images at 1080p and WXGA resolutions. The driver eliminates the need for three discrete laser drivers, allowing system designers to embed pico projectors into new classes of consumer electronics. The driver provides the functions to interface a digital, 10-bit RGB video source to virtually all industry-standard, low-power RGB laser diodes. It includes three 10-bit RGB DACs, reading video data from the host device's 10-bit RGB bus. These DACs allow system designers to control laser current and generate billions of colors and 5000-to-1 contrast ratios. The device suits portable media players, digital cameras/camcorders, and digital picture frames. Available in a 5×5-mm TQFN-40 package, the MAX3600 costs $8.93 (1000).

**Maxim Integrated Products, www.maxim-ic.com**

### Isolated voltage/current detectors have 8-mm creepage and clearance

Suiting use in industrial-control applications, the ACPL-K370 and ACPL-K376 miniature voltage/current-threshold-detection optocouplers detect ac/dc sources, converting the voltage to a logic interface across an optical coupling barrier. The barrier provides safe isolation in the electronically noisy environments that are typical in industrial applications. Representing an upgrade of the vendor's HCPL-0370/3700/3760 optocoupler family, the ACPL-K370 and the ACPL-K376 use threshold-sensing input-buffer ICs. These ICs permit control of threshold levels over a range of input voltages as high as 1140V pk using a single external resistor. Additional features include ±5% voltage-detection accuracy, a 1.32-mA threshold current, a 2 to 18V output-supply voltage, and a −40 to +105°C operating voltage. Available in a stretched SO-8 package with 8-mm clearance and creepage, the ACPL-K370 and the ACPL-K376 optocouplers cost $1.80 and 3.25 (10,000), respectively.

**Avago Technologies, www.avagotech.com**

### LED driver offers temperature-management control

Providing temperature-management control, the LM3424 high-brightness LED driver provides an online design environment and thermal foldback. Designers can program the units' temperature and slope breakpoints, enabling safe operation. The devices drive as many as 18 high-brightness LEDs in series with output currents greater than 2A in a typical application. Available in a thermally enhanced TSSOP-20 package, the LM3424 costs $1.75 (1000).

**National Semiconductor Corp, www.national.com**

# Brown's buzzer busts business


DANIEL VASCONCELLOS

Several years ago, I worked for a company that manufactured professional-grade VTRs (videotape recorders) for use by television stations throughout the United States. The recorders used an arrangement of four heads positioned every 90° on a disk. The recorders pulled a 2-in.-wide videotape past the rapidly rotating disk, and each head recorded about 17 lines of video. The whole thing worked well most of the time because the basic engineering was settled, having been around since 1956, albeit vastly improved by the 1980s when the problem we encountered occurred.

One model used a vacuum-loading system to position the tape in two side-by-side transports for playing commercials. The normal procedure was to initiate a dual-transport load shortly before the commercials would play, using a large rotary storage drum that held 24 cassettes. Additional cassettes would be loaded as the preceding ones were played, rewound, and placed back in the rotary drum.

I was the senior engineer on duty providing telephone support late one afternoon when I received a call from a station. The caller complained that the machine would be happily playing a string of commercials and then suddenly stop in the middle of a sequence. When it stopped, it would ignore the rest of the sequence, rewind the two cassettes previously loaded in the transports, and place them back in the drum. The problem happened only during the station's 6 pm news program. Like with most other TV stations, the station's commercial slots during newscasts were premium placements. The loss of 2 minutes' worth of commercials was a bad thing. The station management was unhappy, which meant that the chief engineer was really unhappy and threatening to drop the VTR off his loading dock into the dumpster.

I pored over the logic diagrams trying to find some failure sequence that could cause the VTR's strange behavior but came up dry. The next day, I boarded an airplane to visit the customer, and, by 6 pm, I was perched on a stool in front of the machine. The first commercial break went fine, but the next one dumped everything midway through the second cassette. There was no warning; it just dumped. Diagnostics found nothing wrong.

During the next day's 6 pm newscast, I began using a four-channel storage scope to probe the logic bay, and the VTR once again dropped the sequence—this time a bit later in the newscast. Again, no clues were present. It was time to recalibrate my approach.

On the third day, I positioned myself between master control and the room where the VTR lived. I could see both the person initiating the commercial playbacks and the machine. I watched closely as the operator initiated each playback. This time, the sequences played fine until the last one, when the machine hiccupped at the precise moment that a buzzer sounded, indicating the arrival of the UPS delivery man on the loading dock. Buzzer sound=machine dump. But why?

As it turned out, the station personnel had run an unshielded twisted-pair remote-start cable from the master control to the machine and placed it in the same cable tray with an equally unshielded twisted-pair cable from a pushbutton on the shipping dock to a high-intensity buzzer. The crosstalk between the two cables was enough to reach the machine's logic circuits and trip the cancel function that shared a multifunction IC with the remote-start function. Had I not gone outside the VTR room and observed the machine dump when the buzzer sounded, I'd probably still be on-site. EDN

***John Loughmiller is manager of engineering for TV One, a television-equipment manufacturer. In his spare time he's a flight instructor who terrifies hapless students.***

# NI LabVIEW

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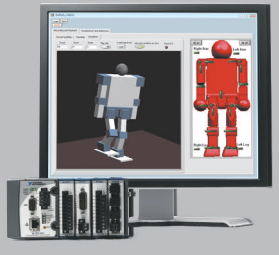
Multicore

LabVIEW graphical programming software and modular NI hardware, such as CompactRIO and PXI, are helping engineers develop fully autonomous robotics systems, including unmanned vehicles designed to compete in DARPA Grand Challenge events.



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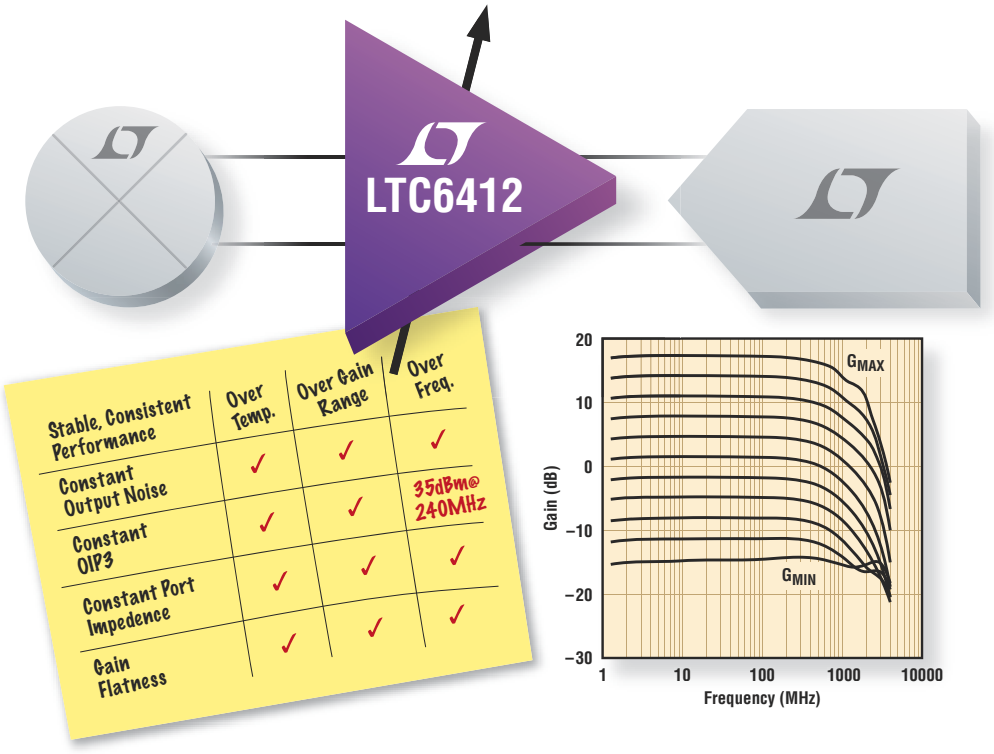
# 800MHz, 31dB Analog VGA




High performance—no compromises. The LTC®6412 is exceptionally consistent across its frequency, gain, and operating temperature ranges. It achieves a noise figure of only 10dB at max gain, and a maximum gain conformance error of 0.45dB. Gain step response time is just 0.4µs. The LTC6412 is powered by a single 3.3V supply and consumes 40% less power than the nearest competitor. The LTC6412 enables a low power, compact solution when paired with low voltage mixers such as the LT5557, ADC drivers such as the LTC6400 and LTC6416, and ADCs such as the LTC2208.

## Linear Technology VGA Family

| | LTC6412 Analog | LT5554 Digital | LTC5524 Digital | LTC5514 Digital |
|---|---|---|---|---|
| **Gain Control Range** | –14dB to 17dB | 2dB to 18dB | 4.5dB to 27dB | 10.5dB to 33dB |
| **Gain Control Step** | Continuous | 0.125dB | 1.5dB | 1.5dB |
| **Bandwidth** | 800MHz | 1000MHz | 540MHz | 850MHz |
| **OIP3** | 35dBm@240MHz | 46dBm@200MHz | 33.5dBm@200MHz | 40.5dBm@200MHz |
| **NF** | 10dB | 10dB | 8.6dB | 7.4dB |
| **Power Consumption** | 363mW | 1000mW | 375mW | 740mW |

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